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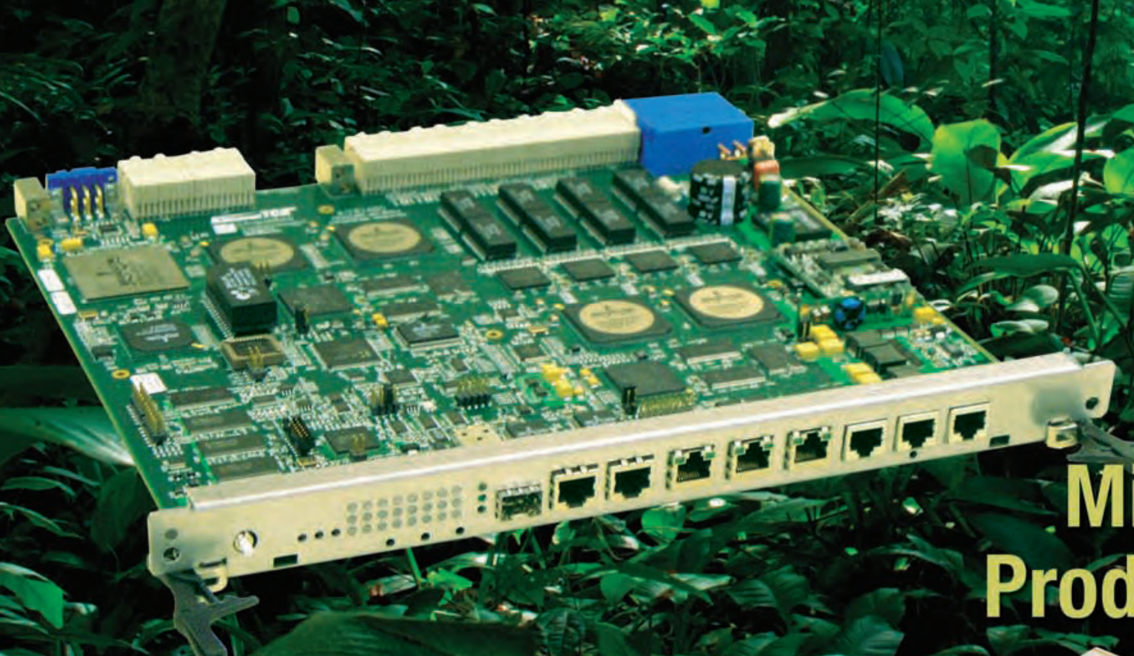
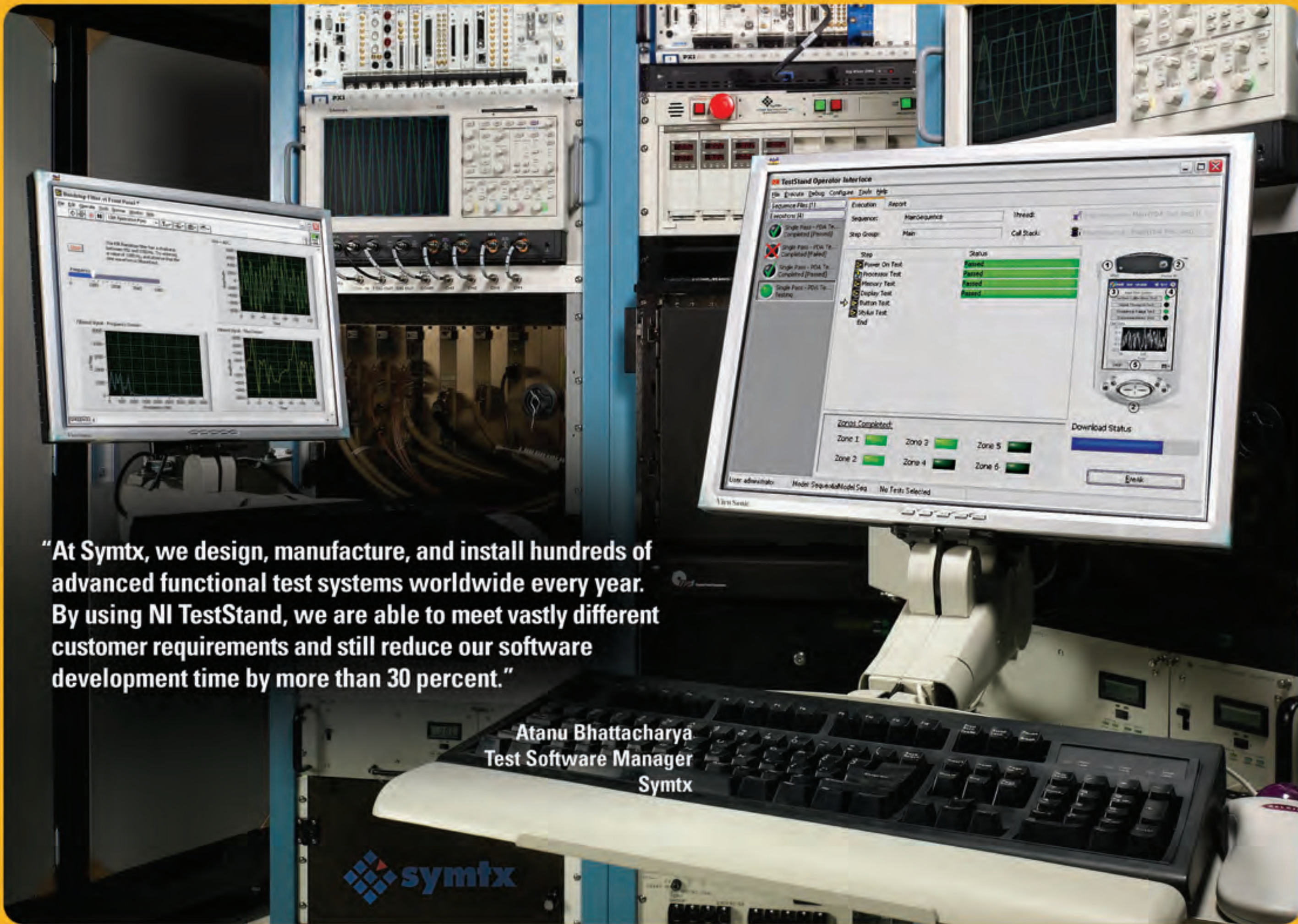
MAY 2006 VOLUME 10 NUMBER 4

AdvancedTCA: Taming the *gotcha!* jungle



Middleware Product Guide

PICTURED
Radstone Embedded Computing
CPX24 Rugged Gigabit Ethernet Switch



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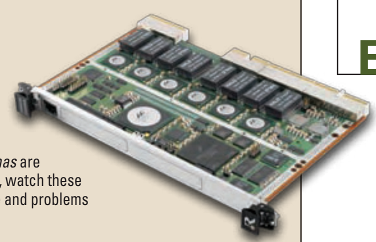

COVER:
The AdvancedTCA specification is a jungle filled with the words *shall, should,* and *may.* It is also a morass of what some call *gotchas.* Although *gotchas* are not problems with the AdvancedTCA specification, watch these *gotchas* for areas where mistakes are easily made and problems often underestimated. See page 24.

CPX24 Rugged Gigabit Ethernet Switch courtesy of Radstone Embedded Computing.

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By Joe Pavlat

Thanks, Guglielmo

The first patent for wireless communications was issued to Guglielmo Marconi in 1896. It used high-frequency *Hertz rays* to transmit signals through the air using a Ruhmkorff Coil (Figure 1). The Marconi Wireless Telegraph Company was founded in 1900 and achieved its first transatlantic transmission the following year. Signaling the end of an era, the company was recently bought by Swedish telecom giant Ericsson AB. It is but one of several recent high-profile industry consolidations, and all signs indicate that more are on the way.

In October of last year Ericsson announced that it was acquiring most of Marconi's businesses, including optical networking, broadband and fixed wireless access, data networking, softswitch technology, and radio. Ericsson will use Marconi's R&D operations to enhance its own IP Multimedia Subsystem offerings. The remainder of Marconi will be renamed Telent and focus on services to enterprise customers and carriers.

Just over a month ago giants Alcatel and Lucent announced they were merging, with Lucent CEO Patricia Russo picked to run the Paris-based company. The deal, which has been widely praised by industry analysts, will give the consolidated company revenues of about $25 billion, compared to Ericsson's $20 billion. After the debacle surrounding the Dubai ports deal, there will likely be some heartburn on Capitol Hill about Bell Labs and their historic ties to the U.S. defense establishment, but the two companies have assured Washington that sensitive military technologies will be placed in independently supervised subsidiaries. A three-person board consisting of former Defense Secretary William Perry, former CIA Chief James Woolsey, and former NSA director Ken Minihan will oversee the Bell Labs subsidiary.

Figure 1

"Each carrier is rushing to provide consumers with a bundle of services – voice, broadband Internet, and video – in what is being called the *triple play*."

In the carrier space, other mergers and acquisitions are making news. The former SBC Communications bought AT&T, and the new AT&T is buying Bell South in a $67 billion deal. Verizon has acquired MCI Inc. What does it all mean?

Making the triple play

First, these consolidations improve efficiency and reduce operating expenses by combining networks. Both AT&T and Verizon have announced plans to make major upgrades to their optical networks in order to prepare for the widespread delivery of video. Each carrier is rushing to provide consumers with a bundle of services – voice, broadband Internet, and video – in what is being called the *triple play*. Carriers and the cable providers will directly compete. Cable providers already offer video and broadband Internet and are starting to deploy voice services in some locales.

While some worry that the glass is half empty and that competition will be reduced, prices will increase, and new equipment purchases will be cancelled, I think quite the opposite is going to occur. The showdown between the cable companies and the telecom carriers will produce the traditional benefits of direct competition for consumers: Better and new services and lower prices. For TEMS, including Ericsson/Marconi and Alcatel/Lucent and their subcontractors, it will mean the deployment of a whole new generation of infrastructure to support the efficient delivery of the bundled services. That will necessitate quick development and delivery of very large amounts of equipment, and that bodes well for open standards like AdvancedTCA, AdvancedMC, and MicroTCA.

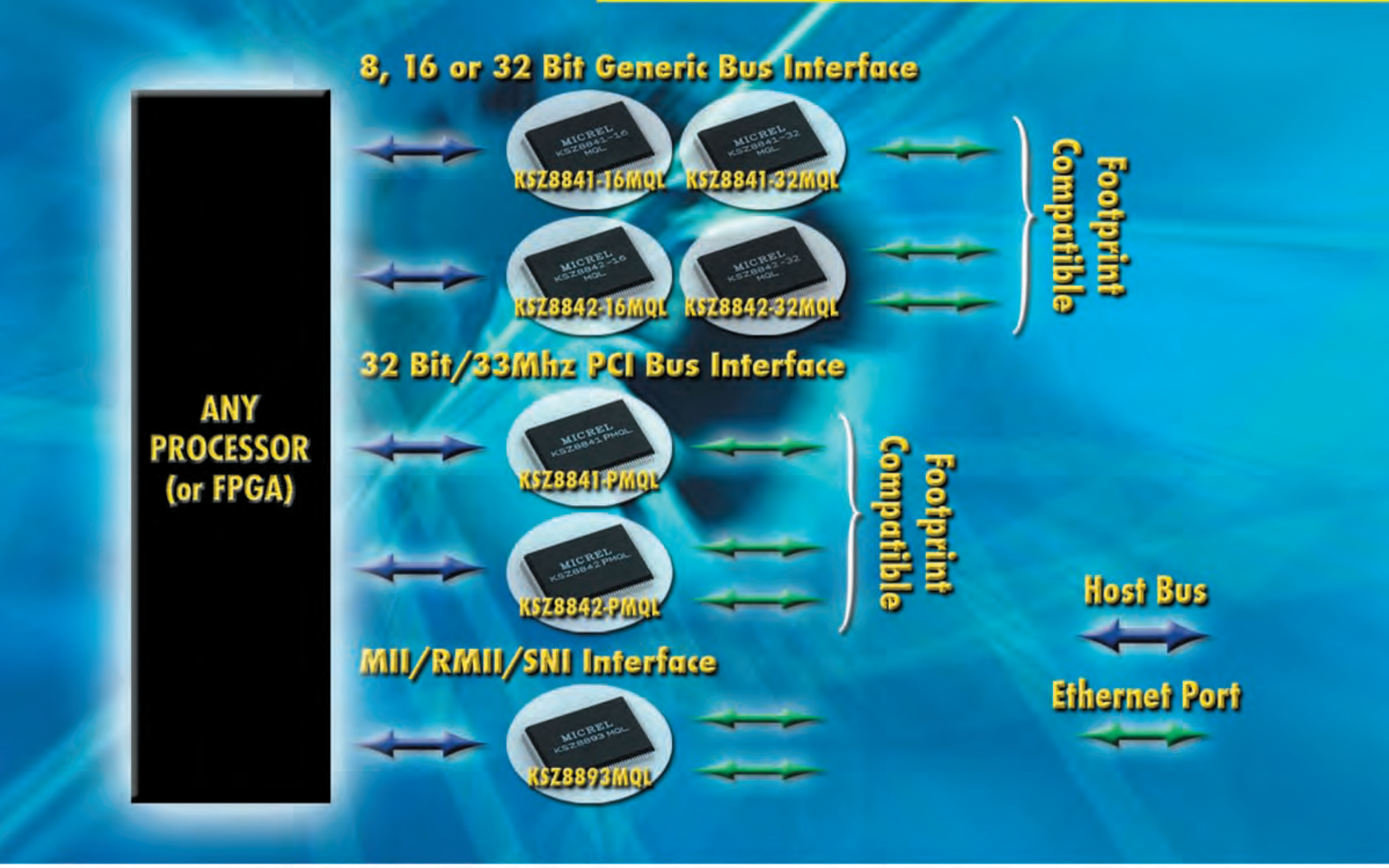
This recent spate of mergers and acquisitions suggests that the communications industry is in for some interesting times. Some will win and some will lose. That's the nature of competition, and we can only hope that Congress doesn't meddle too much. It also demonstrates that the industry is finally recovering from the downturn of a few years ago and looks to be on the upswing. That's good news.

For anyone who is a student of history, I suggest you read Guglielmo Marconi's 1896 wireless patent. It is U.S. Patent Number 586,193 and can be viewed as scanned pages in the U.S. Patent Office archives (www.uspto.gov). Enjoy.

Joe Pavlat
Editorial Director

Embedded Networking?
Micrel Has Your Processor Covered

Micrel's KSZ88xx Series Gives Designers One-Stop Shopping For All Networking Interface Needs



The road to network connectivity is never smooth but Micrel has you covered. Whether you need networking via an 8, 16 or 32-bit generic-bus, PCI-bus, MII, RMII, or SNI host interfaces, Micrel has the answer in easy to install single and dual-port Ethernet solutions. The devices address the growing need for streamlined networking connectivity in IP-Set Top Boxes, VoIP phones, Network Printers, Industrial Controls and networked Game Console applications, to name but a few. The dual port devices have the lowest latency (sub 310nS) in the industry and are ideal for daisy-chaining applications, or simply as two port switches to connect to voice, video and data.

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By Curt Schwaderer

Real-time OS for multicore processors: Serious implications for AdvancedTCA systems

Intel's multicore processor technology has begun to appear in the latest laptop and multimedia PC systems. The technology will also be making its way onto a wide variety of AdvancedTCA system boards for embedded applications. However, without the right software solution for an embedded environment, how successful will the technology be for AdvancedTCA systems?

TenAsys, Beaverton, Oregon has a real-time OS traditionally suited for executing real-time tasks in conjunction with the Microsoft Windows environment on embedded single and multiprocessor systems, and has been validated on Intel multicore processors. This real-time OS, called INtime, works in conjunction with the Windows OS to control real-time tasks while communicating with the Windows environment for graphics and disk support for the non-real-time parts of embedded applications. In this *Software Corner* column, we will be taking a look at the INtime real-time OS and how it operates on these new multicore processors. A big thank-you is extended to Paul Fischer and Kim Hartman of TenAsys for meeting with me to discuss the technical aspects of the solution as well as Bob Patterson of MKTX for coordination efforts.

TenAsys real-time OS history

TenAsys (pronounced ten-AY-sis) has its roots with Intel and the iRMX real-time OS. The iRMX OS was originally developed and maintained by Intel to support the Multibus market. RadiSys Corporation acquired the Multibus business from Intel, which included iRMX. RadiSys Corporation later spun off the real-time OS products as TenAsys was formed.

In addition to the traditional iRMX Multibus business, a new breed of embedded applications began to develop. These new, loosely coupled applications featured an embedded system connected to a Windows PC as shown in Figure 1.

In this loosely coupled configuration, an embedded system running a real-time OS would report back its information to an application running on a Windows PC where the results would be processed, stored, and reported, and where a graphical operator interface would typically be implemented. The devices were coupled through a serial port, shared memory on the same board, or some kind of bus interface, and eventually, Ethernet.

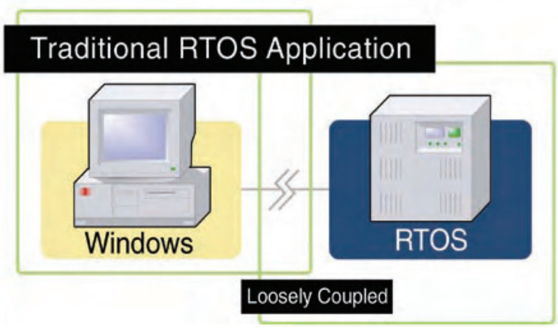

Figure 1

TenAsys created the INtime OS to address the growing business in this area by more tightly coupling the iRMX real-time environment with the general-purpose Windows environment.

The INtime product was launched in 1997. What started in 1990 as DOS RMX (and iRMX for Windows in 1992) changed its API and application memory models so it was more conducive to using tools such as Visual Studio, the preferred development environment for Windows programmers. This transformed many operational aspects but retained, at the heart, the iRMX kernel. The evolution of iRMX to INtime involved enhancements to interprocessor communication, sharing of the I/O interrupts on a system, and changing the real-time OS APIs to provide a rich feature set of I/O and real-time OS capabilities while leaving the graphics and disk subsystems to the Windows environment. While iRMX does have a file I/O subsystem, it is not typically used in the INtime environment, relying instead on Windows for file and graphics I/O.

Intel multicore technology overview

The Intel multicore architecture is as it sounds, two processor cores on the same chip that share the same bus. Intel also provides an on-chip component called the SmartCache, a Level two cache that provides 2 MB of shared cache for both processors and arbitrates between the two. Multicore technology allows the processors to run at lower clock speeds, which reduces the power consumption of the part, another consideration for embedded applications as well as laptops and consumer devices. Other than those items, the part basically looks similar to two processors on a single chip. Memory and I/O are partitioned between the processors, and the traditional multiprocessor board architectures have been shrunk into a single chip.

Real-time and non-real-time processing

Embedded systems of today can typically be broken into two distinct subsystems:

1. The subsystem performing the real-time tasks of gathering information or performing operations that need to meet real-time deadlines
2. The subsystem performing the reporting, storing, and user interface tasks for the application

TenAsys takes the approach that INtime should be optimized for real-time computing tasks with a tight coupling and easy-to-use interfaces that allow Windows to do the information storage, graphics, and user interface displays where it is best suited.

The INtime real-time OS

It is interesting to note that as multiprocessor hardware has evolved from loosely coupled, multiple processors in a card cage to being on the same circuit board, and then finally, to today's Intel multicore processors, TenAsys has followed the same parallels with their real-time OS.

A typical installation model starts with a Windows environment installed in the standard way. Then the memory and I/O resources are partitioned between the two operating environments. Install the INtime real-time OS on the processor performing the real-time tasks for the system. Then bridge the INtime real-time OS with Windows using an NTX DLL on Windows that provides the communication path between the real-time and non-real-time environments.

Figure 2 shows how INtime provides the graphical ability to allocate devices to the real-time environment (INtime) or pass to the Windows environment. All the INtime configuration is done through graphical applications that run on Windows.

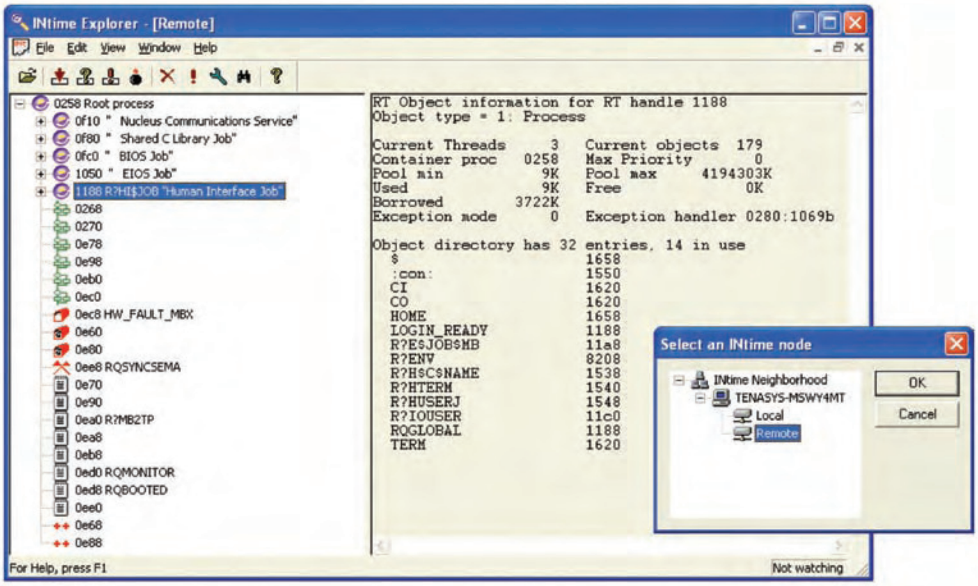

Figure 2

The real-time OS characteristics of the INtime real-time OS present typical real-time OS numbers:

- Less than 10 microseconds interrupt latency
- Multiprocess
- Multithreaded OS
- Real-time network stacks
- Drivers
- Interfaces

The INtime environment has capabilities to allow direct access to hardware I/O programming, which is often important to easy and efficient real-time programming. There are also independent C and C++ real-time-safe libraries. Exceptions are trapped and handled without causing a system crash.

Perhaps the most interesting aspect of the coupling between INtime and the Windows environment is the sharing of the hardware interrupts in the chip. INtime treats the CPU as two sockets. The latest Windows OSs have been written to run in a symmetric multiprocessor environment already, so they are ready for multicore hardware. Hardware interrupts are managed by the *advanced programmable interrupt controller*. The controller includes an I/O controller, with each CPU having a local interrupt controller. The local interrupt controllers work with the main I/O controller to manage interrupts to and from each CPU. The INtime OS takes control of the overall interrupt controller and exposes a *virtual* controller to the Windows environment. During configuration, INtime then handles all interrupts that have been configured for the real-time side of the application and passes through the other interrupts for the non-real-time side of the application through this virtual interface. Additionally, INtime also takes control of the system clock tick in the same manner and exposes a virtual clock interface to the Windows OS.

The NTX layer of INtime does the interprocessor communication between INtime and Windows. It starts with a shared memory partition. Constructs are overlayed on this area to provide high-level constructs for mailboxes, pipes, single/multivalue semaphores, physical shared memory, and mutexes. Signaling between the OS environments uses the interprocessor interrupt capability between the two cores. Blocking and nonblocking communication can be performed through these APIs.

File I/O is done through a pipe interface between Windows and INtime. Therefore, Windows controls the actual file reads and writes for the embedded application.

By coupling the real-time and non-real-time environments, questions may arise as to the impact of the real-time performance of INtime on a multicore processor if the Windows environment gets busy. During my visit with TenAsys, they showed me a demonstration where the INtime OS was performing a real-time task every 30 microseconds. Then various time-consuming tasks were launched on the Windows side. As the Windows side of the dual-core processor got busier and busier, the INtime real-time environment stayed rock solid at 30 microseconds, showing a surprisingly autonomous environment even with the coupling that had been done between the two OSs.

INtime development environment

Perhaps one of the best features of the INtime environment for embedded systems development is how well it is integrated with the standard Microsoft development tools. So, instead of carrying two development environments, the developer uses just one, Visual Studio, to program both the real-time and non-real-time sides of the application.

In addition, INtime enjoys the ability to provide a number of Windows-based diagnostics tools. A couple of these tools are INtime Explorer and INscope.

INtime Explorer is built upon the Windows Explorer paradigm and provides graphical access to all the devices, processes, and threads running within the INtime environment. The Explorer is organized by process space. Each process has a name space containing shared memory and/or objects, similar to how you look at the file system using Windows Explorer. Additionally, properties of these devices and the INtime environment are also accessible through this graphical application.

INScope provides a system-level analysis tool for debugging process, thread, and interrupt interactions (Figure 3). This graphical tool provides the ability to quickly diagnose and fix real-time applications involving sometimes complex interactions between threads, processes, and interrupts that occur during operation.

Developers can also set up markers on a variety of occurrences within the system using INScope to capture tough to debug real-time problems that occur infrequently in the system.

The Visual Studio environment has been extended where TenAsys has provided a plug-in for INtime. For those familiar with programming in Visual Studio, the developer simply does a:

create → project → INtimeRTA or INtimeRSL project.

INtime RTA class is a real-time user mode application. An INtime RSL class is a real-time shared library. The INtime application wizard has a full-featured GUI to create a graphical environment for specifying the resources used by the application. The

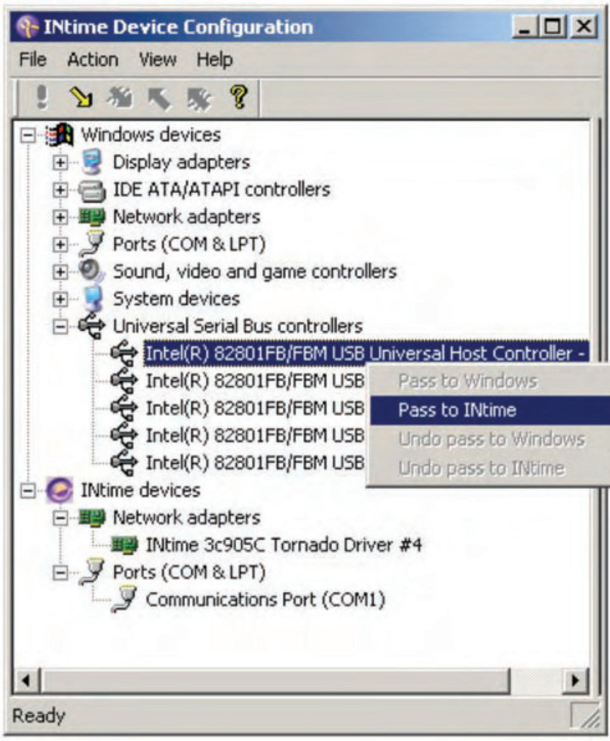

Figure 3

result is a template in C or C++, and it also creates a project in Visual Studio. Visual Studio has the concept of a solution where multiple projects can be grouped. TenAsys uses this facility to wrap the developer's embedded solution into one Visual Studio solution containing Windows and INtime projects.

The Visual Studio debugger has also been integrated with INtime, so traps and exceptions invoke the debugger where you can perform single-stepping, insert breakpoints, and use other standard debugging constructs to debug real-time applications running in the INtime real-time OS environment.

Simulation of INtime applications also becomes a nonissue. Any of the new multicore PC environments can be used as an embedded INtime target machine. So instead of simulating on a sometimes inaccurate simulation environment, you can run the real software on the real OS on a real target, far better than hoping a simulation environment is accurate and up-to-date with the embedded OS you might be deploying.

Other non-real-time environments

So, what if the developer wants to use Linux on the non-real-time side of their application? Intel has been developing a concept with their multicore processor called *virtualization technology*. This technology enables the development of *hypervisor* operating software that can host guest operating OSs. Microsoft has been working toward support of this technology, as has TenAsys. TenAsys is adapting INtime to become a real-time hypervisor, working not only with Windows as it does today, but also able to host other OSs conforming to the interface. TenAsys' solution will interface to any other OS required for the application. Linux is one obvious choice.

AdvancedTCA and CompactPCI applications

What does all this have to do with CompactPCI and AdvancedTCA systems? Look no farther than AdvancedTCA target applications and architecture and see the common ground with INtime embedded applications. Controller cards for AdvancedTCA systems will incorporate multicore processors. Further, the backplane of AdvancedTCA systems and communication with various other cards in the system may require real-time or non-real-time processing. A typical Voice over Internet Protocol (VoIP) application includes the real-time tasks of voice, data, and video stream processing coupled with user interface display. User interface display and input blocking that could impact the real-time performance of the system can be isolated using INtime to control the real-time aspects of the AdvancedTCA system. This kind of software architecture overlayed on the system also applies to areas such as industrial control, medical, and test and measurement systems.

Another interesting aspect to this is the AdvancedTCA architecture and the INtime history with Multibus II. The iRMX real-time OS ability to manage Multibus II systems with backplane message passing could make a reappearance in applications involving today's AdvancedTCA systems.

Conclusion

Most of today's embedded applications involve a dimension of non-real-time graphics and multimedia processing with a dimension of hard real-time processing that must be maintained in order for the system to work properly. Software solutions such as TenAsys' INtime address the need for combining hard real-time responsiveness with general-purpose processing and graphical interfaces with familiar, easy-to-use development tools to shorten design cycles.

For more information, contact Curt at cschwaderer@opensystems-publishing.com.

By Tariq Shureih

A closer look at HPI

HPI in a nutshell

The Service Availability Forum's (SA Forum) Hardware Platform Interface (HPI) specification provides a programmatic API aimed at (1) simplifying the development of system management applications and (2) separating the hardware from the management middleware.

HPI derived most of its concepts from the Intelligent Platform Management Interface (IPMI), which defines a platform independent set of capabilities and data types to manage most any computing system. However, HPI provides an additional layer of abstraction that allows for more generic and broader modeling given the platform has enough management capabilities to be modeled.

An HPI system model comprises domains, sessions, resources, and entities (Figure 1). Domains are containers of resources and entities, and sessions are the basic access method to a system (via the domain container).

Resources and entities are the core data and management access points in systems managed and modeled with HPI. Sensors, control capabilities, status indicators, and inventory data are all associated with a resource in a given domain. HPI provides a complete API to access and control these resources in addition to hot swap, managed hot swap, and chassis power controls. With HPI, you have a standardized API that addresses the heart of system management allowing for quick development cycles and portability.

Open HPI (and it is free)

Open HPI is the Open Source implementation of the SA Forum's HPI. The project has gained much popularity in recent times due to the great success in building a solid HPI implementation based on a modular architecture and bundled support for most popular platform management technologies such as IPMI, Simple Network Management Protocol (SNMP), and less intelligent devices exposed via Linux's SYSFS.

Open HPI was designed from the get-go to be a ready-for-commercial-use open source implementation of HPI. The project is licensed under the revised Berkeley Software Distribution (BSD) license, which allows for reuse and derivatives to the code without the mandate to release the derivative code. Further, the open source can be used with proprietary code without contamination.

After two years of development, Open HPI reached high levels of stability, maturity, and experience elevating it to be one of the leading HPI enablers. That is because Open HPI includes:

- Core library (infrastructure)
  – The core C HPI API shared library providing all HPI interfaces to the user.
  – Plug-in Application Binary Interface (ABI): an internal interface designed for developers to easily write modules for a specific platform with ease.
- Bundled plug-ins
  – IPMI: Both a basic IPMI 1.5 platform support and, just recently, the HPI B.01.01 AdvancedTCA Mapping Specification. This plug-in is based on the popular OpenIPMI library for low level IPMI access and supports rack-mount servers as well as AdvancedTCA.
  – IPMIDirect: This plug-in communicates directly with the Shelf Manager in an AdvancedTCA system over RMCP. It is mainly developed for AdvancedTCA systems.
  – SNMP for BladeCenter: Supports BladeCenter data based on SNMP.
  – SYSFS: Nonintelligent devices such as ADM sensor chips or lm sensors that are exposed via the Linux operating system's SYSFS properties.
- HPI Remoting
  Open HPI also includes an answer to a gap in the HPI specification, which does not address how to transact HPI over remote connections. The specification left it to be implementation specific and Open HPI provides support for lightweight HPI remoting based on client/server concepts. The Core library is used as a client library as well for Management Consoles to access the HPI API. However, in the remoting scenario, Open HPI provides an alternative client library with marshalling combined with an Open HPI daemon running on the managed system to de-marshal the requests coming over the wire.
- HPI View
  – A GTK based HPI GUI application.

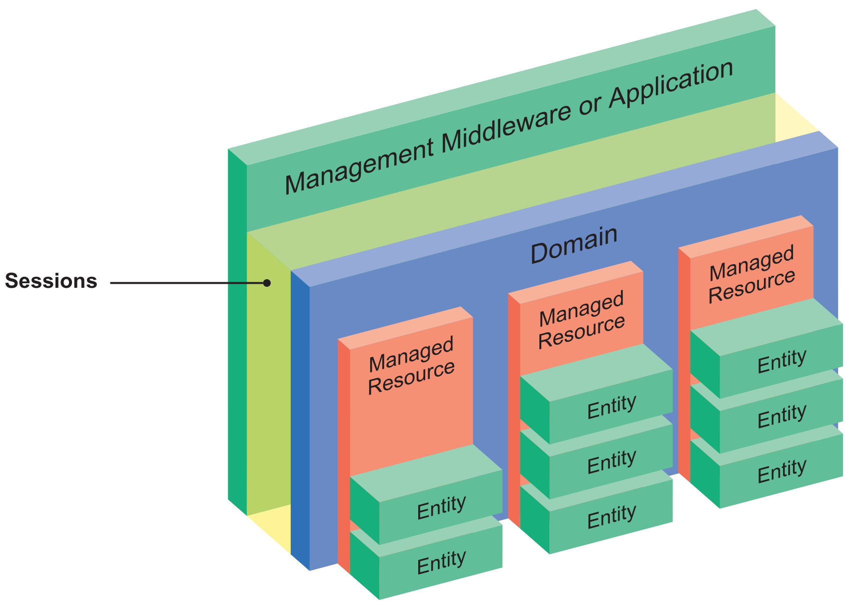

Figure 1

HPI-to-AdvancedTCA mapping specification

The SA Forum provided an additional specification in December 2005 addressing the details of support for AdvancedTCA systems using HPI.

AdvancedTCA is a PICMG standard specifying a bladed chassis with an extensive built-in management capability based on IPMI. In order to address the complexities of a bladed architecture and the expanded functionality, PICMG had to create extensions to IPMI specific for AdvancedTCA to achieve the desired goals beyond those that IPMI 1.5 and 2.0 provided.

Previously, I had highlighted the legacy of HPI in IPMI. However, HPI B.01.01 did not fully expose all AdvancedTCA features and capabilities without further clarification and expansion of the HPI data-types and API. Therefore the HPI-to-AdvancedTCA mapping specification was needed.

Features such as failover, active and standby shelf managers, Advanced Mezzanine Cards, and dual/redundant shelf Field Replaceable Unit (FRU) devices needed to be expanded on or added altogether to HPI in order for implementations to be able to map the AdvancedTCA exposed data using HPI.

The Open HPI Project has been actively developing support for the mapping specification since its announcement, and the work is publicly available in the project's source control (CVS) on SourceForge.

In order to support the HPI B.01.01 and the new mapping specification, Open HPI had to work extensively with the OpenIPMI project. OpenIPMI provides the Linux Kernel IPMI Device Driver in addition to a C Binary Interface to low-level IPMI commands via a shared library.

Conclusion

HPI is becoming a greatly recognized and required interface in the overall telecom and enterprise platform management area. Many Telecom Equipment Manufacturers (TEMs) are requiring that their platform vendors provide integrated support or at least validate HPI (and in most cases Open HPI) support of the platform.

With the introduction of the HPI-to-AdvancedTCA Mapping Specification, the SA Forum strengthened its position as a leader in standardizing the TEM and overall telecom interfaces, thus moving the industry forward and away from proprietary, antiquated, and costly solutions.

The benefits HPI offers its audience are tangible and have been proven over time. Will we see a time when HPI is the de facto interface into a system management? I cannot answer that. However, I predict that HPI will keep growing as market needs increase with the faster and escalating adoption of AdvancedTCA. In addition, vendors are looking for open standards-based solutions and more open source software, and hardware, while platform makers are focusing more on overall platform management.

Tariq Shureih *is staff software engineer in the Open Source Technology Center at Intel Corporation. He has worked at Intel since 1999, and has been the maintainer of the Open HPI project for the past two years.*

To learn more, contact Tariq at tariq.shureih@intel.com.

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By Hermann Strass

Three kinds of control

Image control

To produce high-quality vacation photos for their customers in Europe, AgfaPhoto (Germany) processes film rolls and makes prints to order. The quality of processed photos is influenced by film development and exposure, as well as by paper processing. Digital finishing systems process analog and digital orders with automatic image correction and expose them. High-performance CPU cards (CP605) from Kontron provide functionality and flexibility for the control units. Figure 1 shows a CompactPCI system with a CP605 CPU from Kontron controlling AgfaPhoto's photo lab laser printer machine.

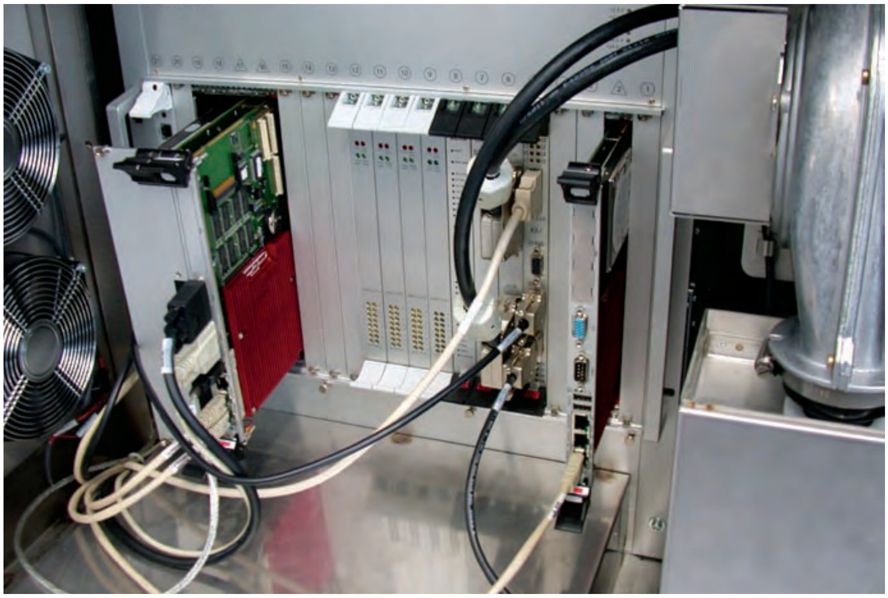


Figure 1

AgfaPhoto develops, produces, and markets laboratory devices, software, and consumer materials for the professional handling and processing of photographic images as well as film and digital storage media for photographs. The AgfaPhoto finishing system, named d-ws, was developed at AgfaPhoto's Munich plant, along with compact digital devices, known as dlabs. The digital high-performance d-ws system consists of several individual components. Features include red eye reduction and alteration of skin tones to be warmer or colder.

Film rolls are digitized on the d-scan.20 high-performance scanner and processed with the digital Total Film Scanning (d-TFS) image optimization software and other optional processing algorithms. The corrected image data files are then provided to the d-print.20 high-performance printer, which exposes them onto roll paper at a speed of 49.4 meters per minute, which is approximately 150 feet per minute.

The mobile Pentium 4 M processor used by AgfaPhoto on the CP605 CPU operates at a frequency of 2.2 GHz. Passive cooling is sufficient for all processor variants. Thermal management prevents overheating even under unfavorable housing and system conditions. The unit's high-performance scanner contains two CP605 CPU cards. One CPU card has been modified by Kontron to include a storage module with DVD drive and 3.5-inch hard

drive. The CPU and storage module form a compact unit, which can be removed as a complete module for service. Kontron delivers this expandable module fully mounted and tested to AgfaPhoto. The printer and exposer are controlled by other CP605 cards. The machine control runs under Linux, because it is more economical and more secure than a Windows operating system in terms of cost and real-time capability. Windows 2000 is used for the image processing.

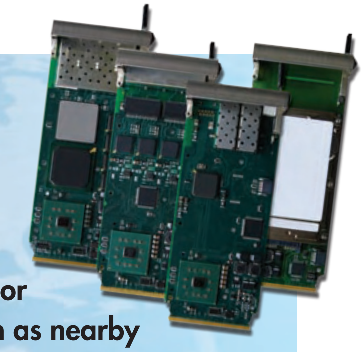
Heat control
Concurrent Technologies (UK) has released a board for AdvancedTCA systems. The PR AMC33x mezzanine board features many AdvancedMC-defined interfaces and functions. It will operate at temperatures up to 55 °C in fanless mode using a 2 GHz Pentium M processor, and offers 2 GB of ECC memory. This lead-free AdvancedMC module complies with:

- AMC.0 (hot swap, SW, FH, IPMI V1.5)
- PCI Express x8 (AMC.1 Type 8, Rear I/O)
- Gigabit Ethernet (two AMC.2 Type E2)
- SATA (two AMC.3 Type 2)

All components, including memory and processor, are soldered lead-free for higher Mean Time Between Failure (MTBF) and improved deheating. It supports Windows, Linux and Real-Time Operating Systems (RTOSs), QNX, and VxWorks.

Remote control
Pickering Interfaces (UK) has introduced a LAN eXtensions for Instrumentation (LXI) chassis that is fully compliant with Functional Class C of the LXI standard. The chassis accepts any of the more than 500 3U PXI modules from Pickering Interfaces. Engineers can install and control these modules through a standardized LXI Ethernet interface. The 60-100/101 chassis (7/13 slots versions) permits users to choose Pickering PXI products regardless of whether the test system is working in a PXI or LXI environment. The LXI-compliant Ethernet interface permits the chassis to be controlled through standard LXI Ethernet interfaces. It allows the remote operation of test and measurement systems with simple cabling to be controlled over worldwide networks. Separation of the chassis from the PCI bus of the controller provides a high degree of independence from the Windows environment.

For more information, e-mail Hermann at hstrass@opensystems-publishing.com.



CES (Switzerland) has developed four AdvancedMC mezzanines, one OC3, and two different Ethernet modules and an AdvancedMC that can hold a SATA 2.5-inch hard disk. CES is delivering boards and systems, mostly based on CompactPCI, VME, or PCI Mezzanine Card (PMC) to institutions such as nearby CERN, the European Laboratory for Particle Physics, and to all major aerospace companies. Many deployed systems use LynxOS (DO-178B and POSIX compliant) as an RTOS.

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Implementation of an AdvancedTCA/ MicroTCA-compliant congestion management architecture

By Will Chu and John O'Day

In this article, Will Chu, President, CorEdge Networks, and John O'Day, Director of Technical Marketing, Celestica Communications Design Practice, discuss the need for a highly flexible 10 Gigabit Ethernet system in telecom systems with hardware-level congestion management to deliver a high-performance and manageable system.

Two separate but related megatrends currently exist in the telecom equipment industry. The first is the adoption of AdvancedTCA and MicroTCA (or on a combined basis, xTCA), which most Telecommunication Equipment Manufacturers (TEMs) are adopting for their next-generation architectures. xTCA promises to lower costs and speed time-to-market by freeing TEMs to focus on system architecture with high-value, high-layer software without the need to develop lower-layer, lower value-add infrastructure hardware and software from scratch. On the other hand, xTCA offerings to date have largely been designed with basic microprocessor blades that are good at doing data center-type computing tasks, but which are less equipped to handle heterogeneous networking wirespeed flows at 10 Gbps or above without interruption. These early implementations do not leverage the terabit capabilities that xTCA systems are able to deliver, and this has slowed the adoption of xTCA for next-generation telco networks.

The second megatrend is the need for wirespeed congestion management in order to deliver high-performance, scalable, and manageable systems across the network. This is becoming particularly important as wireless service providers begin to deploy 3G IP Multimedia Subsystems (IMS) that support voice, data, and video. At 1 Gbps speeds, supporting latency-sensitive quality of service is possible with software solutions. At 10 Gbps and above, the management of the network needs to be pushed down into lower-layer hardware, as software on microprocessor blades will be hard pressed to keep up with a network changing at 10 Gbps. Latency-sensitive applications such a voice and video will share the same physical infrastructure as less latency-sensitive data traffic, requiring the networks to manage traffic and congestion intelligently. When a single system is handling thousands of users, each with multiple megabits of data per users, the system quickly needs to handle multiple gigabits of data.

Unfortunately, until now, mainly expensive, proprietary techniques and hardware could support such wirespeed congestion management. To develop a lower cost, standardized mechanism for congestion management at Layer 2 over Ethernet, the 802.3ar committee has been established within IEEE, with members that include many of the world's tier one OEMs in telecommunications, semiconductors, and networking. It hopes to develop flow control standards for Ethernet by early 2007.

With a goal of assisting this standards effort, a group of companies from within the 802.3ar and xTCA efforts, CorEdge Networks, Celestica, and Fujitsu, a tier one TEM, along with other companies participating in future designs, partnered to create a prestandard implementation of wirespeed flow control, using xTCA form factors. The goal of this effort was to create a COTS implementation for this kind of equipment using AdvancedTCA-compliant equipment at the network core, and MicroTCA equipment at the edges, with AdvancedMC cards used ubiquitously.

The architecture was designed to meet several critical design requirements. These included:

Backplane fabric choice
The AdvancedTCA specification defines a number of backplane protocol and topology choices, and choosing the right set is a function of the features needed in a given application. From a protocol standpoint, the group decided to use Ethernet due to its low cost and universal deployment, scalable access speeds, and because it offers the best combination of technical characteristics and interface controller availability. Furthermore, moving to 10 Gigabit Ethernet (XAUI) for the fabric switch allows for a high-performance solution that ensures bandwidth is available to meet TEMs' future needs.

AdvancedTCA backplane topology

In terms of the backplane topology, PICMG specifies three options. The group chose the full mesh option as an effective choice for this application since it provides advantages in system scalability, system redundancy, and physical efficiency.

AdvancedTCA carrier card

For core AdvancedTCA switching, an AdvancedTCA carrier card was built that uses high-capacity XAUI fabric switch silicon supporting 60 SERDES lanes (4 lanes for 15 nodes) per AdvancedTCA blade. An example of this type of board is seen in Figure 1. It can mount two AdvancedMCs, with a 24- port XAUI switching fabric. The carrier card was designed by Celestica, using Fujitsu 10 Gigabit Ethernet switch chips and CorEdge Networks' IPMC. Customers developed the software layer required to deploy this solution for the customers' specific applications.

Figure 1

MicroTCA Carrier Hub (MCH) and fabric

For the MicroTCA system, the MicroTCA Carrier Hub (Figure 2) from CorEdge Networks was used along with an MCH fabric card that also used the Fujitsu switch chip.

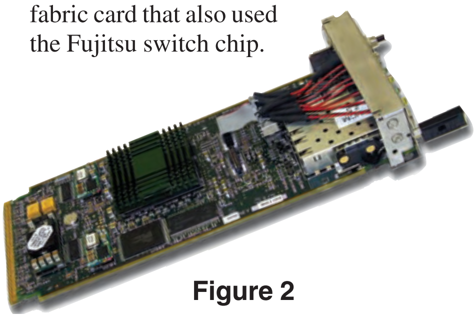

Figure 2

AdvancedMC/AdvancedTCA/ MicroTCA interoperability

A critical consideration when designing an architecture for congestion management across a wide range of packet types and network applications (and with different boards designed by different vendors) is interoperability. Creating such a solution requires *bridge* silicon that handles multiple protocols (SPI4.2, GMII, RGMII, PCI/PCI-X, PCI Express, 1 Gigabit Ethernet, 10 Gigabit Ethernet, RapidIO, and Serial RapidIO) so that it becomes a generic interface for application-specific silicon that does not have 10 Gigabit serial native interfaces (for example, NPU, Microprocessor, Security, Semantic Processing, and DSP). This bridge silicon also must support popular telco backplane protocols (1/10 Gbps Ethernet and Serial RapidIO) so that AdvancedMCs can become reusable in Ethernet or Serial RapidIO applications and in both AdvancedTCA carriers and MicroTCA.

The bridge silicon used in this project was developed by CorEdge Networks, and is designed to provide Ethernet Layer 2 hardware based flow control using IEEE 802.3ar techniques to provide guaranteed packet delivery and congestion management at low latency at 10 Gbps using Ethernet. For this demonstration, several CorEdge Networks 10 Gbps AdvancedMC Line Cards (Figure 3) were used.

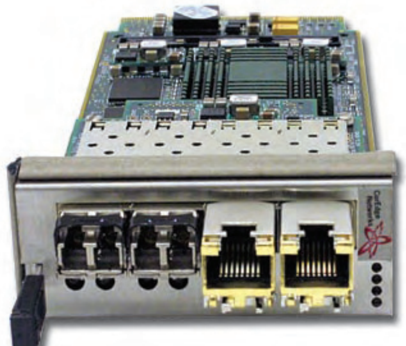

Figure 3

The CorEdge Networks bridge chip and IPMI MMC solution are also being used by third parties to develop next-generation AdvancedMCs that will interoperate within the overall architecture. These next-generation AdvancedMCs use different application silicon (NPU, Microprocessor, Security, Semantic Processing, and DSP) in conjunction with the bridge silicon so that they are enabled with 10 Gigabit Ethernet (XAUI) with IEEE 802.3ar hardware flow control.

At GLOBALCOMM 2006, a working version of this architecture will be demonstrated at the PICMG pavilion. Streaming video from a source laptop (along with a second-source 10 Gbps data

stream) will go into a MicroTCA chassis, then switch through an AdvancedTCA switch, into a second MicroTCA chassis, and then play on a second laptop. When flow control is engaged, the video stream comes through without degradation. However, when flow control is disengaged with the second 10 Gbps data stream contending with the video for priority, the video becomes unwatchable.

We believe that this first working demonstration of a prestandard IEEE 802.3ar network in an xTCA-compliant form represents a milestone for the telecom industry, and we hope that it spurs accelerated adoption of the IEEE 802.3ar standard.

***Will Chu** is the president of CorEdge Networks, a leading developer of AdvancedTCA, MicroTCA, AdvancedMC, and IPMI products, and he helped to start the company in 2004 while he was a principal at Signal Lake Ventures. At Signal Lake Ventures he focused on early stage venture capital investments since 2001. Prior to that, he held various technical and managerial positions at Fidelity Investments, Texas Instruments, ITU Ventures, and a number of startups. He holds an MBA from the MIT Sloan School of Management and graduate EE degree from Tufts University.*

***John O'Day** is the director of technical marketing for Celestica's Communications Design Practice, of which the company's building blocks for AdvancedTCA systems and boards for Celestica's design services are a part. Prior to joining Celestica, John worked with Arrow Electronics. Throughout his career, John has held roles in technical marketing, business development, sales, and product management in the embedded computing market – all relating to embedded and high-performance computing in VME, CompactPCI, and most recently, AdvancedTCA.*

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Welcome to the jungle (of AdvancedTCA *gotchas*)

As a kid growing up, I have vivid memories of watching Tarzan movies after the Saturday morning cartoons were over. We only had three channels, so we didn't waste a lot of time channel surfing. You watched what was on and you liked it. In about half of those Tarzan movies, you had the bumbling man wearing a French pith helmet or topi. This poor soul would be hacking his way through the jungle with an oversized, extremely sharp machete. Unknowingly, he was facing almost certain death via a lion or some other jungle-induced demise. A couple of badly sequenced movie cuts later and topi man would be dead. A required extermination, so a vine-swinging Tarzan could rescue the completely bewildered people who had been following the recently dispatched soul. As a kid, I remember feeling sorry for this man. He did all that work, and the people following him did nothing, yet his reward was death.

The AdvancedTCA specification is a jungle filled with the words* shall, should, *and* may. *It is also a morass of things that I like to call* gotchas*. These* gotchas *are certainly not problems with the AdvancedTCA specification, but they are areas where mistakes are easily made and problems are often underestimated. Therefore, I will now don my helmet, raise my machete, and attempt to cut through some of the more obvious* gotchas *that are ahead in the AdvancedTCA jungle on our path to the prosperous Land of Revenue.

By Joe McDevitt

As we near the edge of the jungle, a great thorny thicket called electronic keying exists. Since AdvancedTCA (Figure 1) is a fabric-agnostic architecture, an interesting set of design requirements arises. A major one is the relative ease in which dissimilar fabric technologies could be inadvertently connected. In the non-AdvancedTCA world, differing cables and connectors help to alleviate the issues of putting dissimilar fabrics on to the same physical interface. In AdvancedTCA, those cables are replaced with a backplane featuring common connectors; therefore, a new method for preventing accidental fabric interconnection is needed.

The AdvancedTCA specification relies on electronic keying, or E-keying, to prevent these issues. The Shelf Manager knows which slot each board is in, each board's fabric, and the backplane connectivity, so it is an arbiter among the boards and determines which boards' fabric ports can be turned on. The Shelf Manager tells a board to turn off its fabric ports when dissimilarity is found, and that board must disable transmit functionality on its fabric ports.

The *gotcha* lies in how this disabling is accomplished. On some AdvancedTCA boards that ship with a software application, E-keying support can be easily assured. On generic AdvancedTCA boards where no such application exists, who has the ultimate responsibility to disable transmit on the fabric? If chip vendors do not provide a way to disable the transmit SERDES on their chips, then how can handcuffed engineers meet the requirements of E-keying while maintaining the eye pattern requirements of the fabric? E-keying issues are not insurmountable, but like going through a thorny thicket, even armed with a machete, getting through the issues will involve torturous tasks.

Figure 1

PEM solutions

Passing through the thicket, we spot a well-worn path. A little farther down the path, we notice a tree with a large hole dug into the side. The edges around the hole make it clear this is the spider hole for the venomous hold-up capacitor spider. The hold-up capacitor spider will attack anything passing by the hole and bite it, leaving a pain that will last until the next board revision. But if the hole is seen, the bite is easily avoidable. The hold-up capacitor requirement is likely an old *gotcha*. Many Power Entry Module (PEM) solutions exist today that address specific needs for AdvancedTCA and all of them recognize the need for a hold-up capacitor.

In the early days of AdvancedTCA, these targeted solutions didn't exist, and a few words buried deeply in the specification, almost hidden, drove the hold-up requirement. Years ago, some prototype boards at early AIW conferences could be seen without the required capacitance. Today, the *gotcha* has likely been reduced to the physical size of the capacitance needed. The application schematics for targeted PEM solutions certainly show the hold-up cap, but the size of the schematic symbol almost never does justice to its physical size.

Engineers who are accustomed to specifying components for digital circuits can lose sight of the fact that this is a huge capacitor. This capacitor can be measured easily in square inches of board space, and the layout engineer is sure to feel some of the bite anyway. Dividing it up helps, but it is still lost board real estate. Carefully

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look for the hold-up capacitor spider hole and beware its venomous bite; once seen, it is easy to avoid.

Our jungle path comes to an intersection and diverges into many roads. Each road is different, and all seem to promise dangerous obstacles, both seen and unseen. A granite obelisk in the middle of the intersection has these words engraved:

"Choose a handle solution."

Like the hold-up capacitor, this may also be a *gotcha* that has passed its time. However, Diversified Technology, Inc. (DTI) has used no less than 11 different handle solutions, covering the almost four years and 10 unique AdvancedTCA products that have been developed since DTI's first AdvancedTCA prototype. Many of those changes obviously occurred because of the newness of AdvancedTCA, and the industry dealt with problems no one foresaw along the way. But the *gotcha* of market consolidation may remain. With the breadth of handle solutions available today, which ones will last throughout the planned length of a company's AdvancedTCA deployment is unclear. With no electrical switch locations or switch types defined in the specification, this seemingly adds a requirement of signed contracts from sole source handle vendors for assurance of five-year availability.

AdvancedMC sites may or may not be another dangerous obstacle that could force us all the way back to the granite obelisk, where we must choose our path again.

"AdvancedTCA testing represents a set of obstacles and decisions that require some preplanning."

The labyrinth

After we clear the handle obstacle course, our path leads to a small grassy knoll. Here before us lies an old stone walled labyrinth, thick with growing vegetation and creepy things inside. From this vantage point, it is not clear which path is the correct one through the labyrinth, but obvious wrong ones can be seen. As we approach the massive stone walls, a simple sign above the entrance says "Testing." All testing in AdvancedTCA will be different. From the first simple stress tests on a prototype to final production line testing, AdvancedTCA testing represents a set of obstacles and decisions that require some preplanning. Consider a simple Ethernet traffic generator and exerciser. Nearly all these test devices assume a BASE-T or RJ-45 type of Ethernet connection. With AdvancedTCA base fabric, this is a simple conversion matter. However, the problem is much more difficult on the expansion fabric of AdvancedTCA 3.1, because it uses BASE-BX; this means that an Ethernet PHY is required to interface to existing network equipment. The testing problem doesn't end with prototypes, either: Production line testing may need specialized backplanes with nontrivial development. No company is immune, and they all will have to plot their own course through the testing labyrinth. As with a maze, the more times one goes through the testing problem, the easier it becomes, but some cautious planning from the grassy knoll before entering the labyrinth can always save a few wrong turns.

Upon exiting the testing labyrinth, we spot the indigenous Marketing tribe dancing around a fire, seeking supreme guidance from their requirements idol. With CompactPCI and PICMG 1.0, space was always the deciding factor on which marketing requirements would make it onto a board. The AdvancedTCA specification limits a board to 200 W at the entry point. With modern digital silicon, -48 V at the entry point must be converted to a more usable voltage. If the front-end conversion of this entry voltage is 90 percent efficient, then only 180 W of power remains. That is not much power with today's

digital silicon. While this is sufficient power to handle processors and certain memory sizes, the number of AdvancedMCs and other devices on boards can become an issue. Usable power, not historical space issues, can quickly limit the final feature set of a board. Ultimately, this specification requirement alone will reduce the differentiation of some higher-level boards. Power limitations will simply not allow any differentiation. The market will be driven even closer to *form follows function* design. For the AdvancedTCA customer, beware of boards that are functionally the same but have apparent radical differences; for example, the number of AdvancedMC sites. For my hardware brethren, beware of those marketing natives. They will be restless when they see large amounts of green PCB apparently going unused, as this offends their requirements idol.

We will rest now and set up camp next to the indigenous Marketing tribe. A few guards will be posted because I'm not sure if this Marketing tribe is cannibalistic or not. I think we have appeased them with a time to market trinket, so it should be safe. We are closer to our final destination, the Land of Revenue. After our guided tour through a portion of the AdvancedTCA specification's jungle of *gotchas*, maybe now your path to production is slightly clearer for your design. Perhaps you've concluded that the author of this article is really just that bumbling man in the helmet. In closing, I leave you with a few words of caution. If you are one of those unprepared, bewildered people following me, Tarzan was a fictitious hero, and there aren't any swinging vines in the AdvancedTCA specification. Hey, look! On the edge of our campsite is the rare NEBS Compliance lion. Man, he looks mad.

Joe McDevitt *started his career with Diversified Technology, Inc. in 1995. He has dual BS in Electrical Engineering and Aerospace Engineering from Mississippi State University. As a hardware engineer, Joe was a lead engineer on the development of several symmetric multiprocessor servers specifically designed for telecommunication markets. Joe was promoted to Hardware Engineering Manager at DTI and spent several years overseeing the development of many of DTI's processor products. Joe is now DTI's VP of technical development, assisting and managing the development of products using new technology and other cutting-edge products like AdvancedTCA and AdvancedMC.*

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Selective memory: Keep these 10 considerations in mind for AdvancedTCA blade design

By Arthur Sainio

2006 is shaping up to be the year for AdvancedTCA blades. The telecom industry is adopting open standards-based building blocks in place of proprietary systems, and AdvancedTCA blades will likely be the form factor of choice for next-generation carrier grade communications equipment. While AdvancedTCA blades have a standard architecture, they do not have standard memory requirements. Designers choosing AdvancedTCA blade memory need to consider many options and weigh the design/cost trade-offs carefully. Here are 10 key considerations to keep in mind when planning an AdvancedTCA blade design.

1 Technology type

For AdvancedTCA blades, the two main memory choices are DDR1 or DDR2 (Figure 1 shows DDR2 modules). The market transition to DDR2 is happening now; however, DDR1 still has a long life ahead. Typically the memory technology decision depends on the processor and chipset, but it is helpful to consider product life cycles and where they align with memory trends.

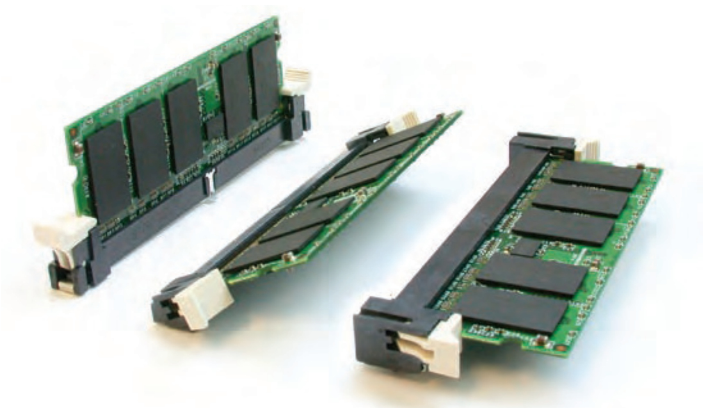

Figure 1

2 Form factor

The increase in AdvancedTCA-standard blades has led to a wider variety of available small module solutions. Table 1 shows the best module types for AdvancedTCA blades.

3 Configuration

The processor and chipset interfaces typically define module configurations, but designers can usually select from registered, unbuffered, unbuffered with ECC, and unbuffered with ECC/PLL clock driver. With unbuffered memory, the chipset interfaces directly with the memory, whereas with registered memory, registers hold data for a defined number of clock cycles.

After determining the module type, it is time to select a configuration. Common module data widths include:

- x72
- x64
- x32
- x16

Multiple DRAM combinations support these configurations.

4 Connectors

Currently, there are four basic connector options:

- Vertical
- Right angle
- Horizontal (notebook type)
- Angled

With AdvancedTCA blades, it is common to use 244-pin right angle mini-DIMM connectors that allow for low height as well as space underneath for extra passives. Vertical connectors in combination VLP modules can also be used to save board space and meet sub-1U height requirements. Finally, butterfly pairs of SODIMM connectors can be used to achieve high density and still accommodate a mezzanine card on top.

5 Power consumption

When evaluating the thermal efficiencies of memory subsystems, consider such factors as DRAM power consumption, system airflow, DIMM pitch, DIMM thickness, and whether a heat sink will be required. Power consumption will vary depending on the type of DRAM, but using modules designed with 8- or 16-bit wide DRAMs can typically lower consumption.

Technology	Module Type	Max. Density	# of Pins
DDR1	VLP Registered DIMM	4 GB	184
DDR1	SODIMM – Unbuffered, ECC	2 GB	200
DDR1	SODIMM – Unbuffered	2 GB	200
DDR2	VLP DIMM – Registered	4 GB	240
DDR2	Mini-DIMM – Registered	2 GB	244
DDR2	VLP Mini-DIMM - Registered	1 GB	244
DDR2	Mini-DIMM – Unbuffered	1 GB	244
DDR2	VLP Mini-DIMM - Unbuffered	1 GB	244
DDR2	Mini-DIMM – Unbuffered, ECC	1 GB	200
DDR2	SO-CDIMM – Unbuffered ECC	1 GB	200
DDR2	SO-RDIMM – Registered	1 GB	200
DDR2	SODIMM – Unbuffered	2 GB	200

Table 1

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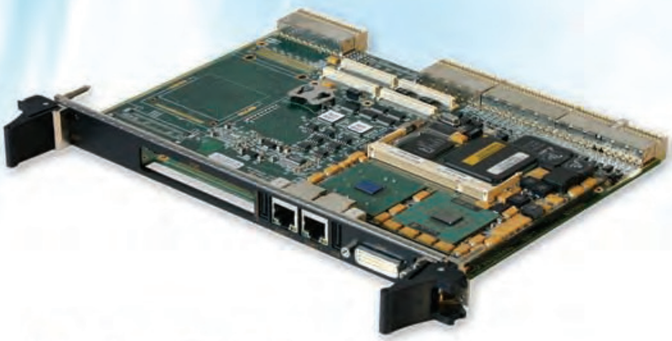

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- Four USB-2.0 ports and two serial ports
- 1600 Gate user configurable CPLD, with 32 GPIO lines
- Up to 512KB of BIOS/user Flash
- RTC with field-replaceable battery
- CPU temperature and voltage monitoring for safe operation
- Fully Hot Swappable 64-bit/66MHz CPCI bus
- Available in standard 0°-55°C or extended temp. -40° to 85°C
- Support for Windows® XP/2000, VxWorks® and Linux®

*Also available in VME

S620 "HAWK"

Mini-ITX with Dual PMC Pentium® M System

- Ultra small footprint system, Only 2" x 7" x 10" and 4.5 lbs.
- Up to 2GHz+ Intel Pentium® M processor with up to 2MB of L2 Cache
- Field upgradeable CPU module to deploy latest Pentium® M processors
- Ultra-low power requirements as low as 10W max
- Up to 2GB of 266MHz DDR SDRAM
- Dual Gigabit Ethernet with TCP/IP Offloading Engine
- High performance dual video display (RGB and DVI) with 64MB RAM
- Dual Video to support two DVI monitors or DVI & RGB together
- 2D/3D video acceleration with OpenGL® and Direct-X® support
- Two PCI-Mezzanine-Carrier (PMC) sites for high-speed I/O expansion
- Dual channel Line-In/Out/Mic with CD audio for full Multi-Media support
- Dual 1394A and quad USB-2.0 ports via front/rear I/O panels
- Ultra quiet fan for Desktop applications
- Full power management control:
  - -ACPI 1.0 compliant (suspend to memory/disk etc.)
  - -Geyserville® III support (speed and voltage stepping)
  - -Support for battery operation and standby power
- CPU, system temperature and voltage monitoring for safe operation
- Up to 100GB ATA HDD and CD-RW/DVD±RW Drive
- Support for Windows® XP/2000, VxWorks® and Linux®

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FILE NUMBER A8073

6 Density

Packet-processing AdvancedTCA blades typically require lower density ECC modules while network appliance type of AdvancedTCA blades require 2 GB to 4 GB registered modules. BGA package size variations directly affect module form factor cost and the need for stacking options.

7 Price

Memory modules are a cost-effective design option because they can be changed to accommodate prevailing DRAM densities and prices. The key is to make sure the system is designed to function with the widest set of options, including support for 1 Gb devices, faster speed grades, and single or multiple ranks. The idea is to set the basic systems priorities first (for example, performance, low power) then work to achieve the best cost efficiencies.

8 Standard or derivative modules

Derivative modules follow the JEDEC pinout and socket standards but have been customized to meet specific customer requirements. These requirements include reducing clock loading, adding an extra chip select so the density can be upgraded by stacking, and moving far-end termination onto the module to save board space. Derivative modules shorten design cycles and development costs as compared to fully custom memory modules, yet they allow system designers to gain competitive feature advantages.

9 Testing

Increased processor speeds, more processors, and larger memory capacity combined with decreased board space and reduced air-flow have resulted in systems that run hotter and are more prone to single and multibit memory errors. Choosing modules with ECC and designing systems that support Chipkill can minimize the impact of memory errors on system functionality.

10 Trade-offs

Choosing memory demands careful consideration among all trade-offs: Cost, thermals, capacity, connector type, spacing, module form factor, and configuration – all need to be weighed based on the application and market requirements However, with careful planning, AdvancedTCA designers can get the most out of their memory choices.

__Arthur Sainio__ is responsible for new product introduction and technical support program development at SMART Modular Technologies. He has been at SMART for more than seven years. He previously worked for six years in flash, DRAM, and SRAM product marketing at Hitachi Semiconductor America. He holds an MBA from San Francisco State University and an MS degree from Arizona State University.

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Bridging the management and availability gap for AdvancedTCA

By Raju Penumatcha

To survive in today's highly competitive telecom equipment market, Telecom Equipment Manufacturers (TEMs) must rapidly deliver cost-effective solutions for deploying and managing next-generation voice, video, data, and Internet services across a wide range of networks. One element of their strategy is to use more standards-based, Commercial Off-the-Shelf (COTS) technology, such as AdvancedTCA, to reduce development costs and speed time to market.

In addition, emerging system management and High Availability (HA) standards from PICMG, SAF, DMTF, and others are simplifying the development of cost-effective, interoperable element management systems. In the descriptions found in the Middleware Product Guide *that follows, you will find references to implementing SA Forum HPI and AIS interface specifications, SAF-compliant HA middleware that allows the telecommunications OEM to easily develop a media server, and interwoven software modules and APIs that provide middleware services for HA telco applications.*

Standards come up short

The arrival of AdvancedTCA telecom blade architecture is ushering in a new era of cost efficiencies and rapid time-to-market capabilities for the telecom industry, but these gains can be quickly eaten away by the extensive heuristic coding required to provide the comprehensive element management system and all-component fault coverage needed to meet extremely high service levels demanded by service providers and end customers alike.

Despite tremendous progress, standards from PICMG, SAF, DMTF, and other standards bodies fall short of meeting all management and availability requirements for AdvancedTCA blade platforms. For example, no mechanism seamlessly shares hardware monitoring information provided by an AdvancedTCA-compliant fan to the SAF HPI, as the emerging standards fail to specify rules for applying system management specifications based on information models.

The lack of an integrated element management architecture across all heterogeneous network elements creates another gap. For example, consider a power failure in an AdvancedTCA chassis. The administrator receives notification of failure from the shelf manager, but the current standards do not identify the exact source of the failure. Is it a bent pin in the slot, an overloaded power zone, a blown fuse in the power entry module, or a problem with the main power feed inputs? The administrator wastes time attempting to isolate the source of the fault and may even send a component back to the TEM, only to have *no trouble found.*

Thus, despite tremendous progress in standards, TEMs must still expend considerable time and effort developing an overarching element management architecture that unifies these standards into a comprehensive element management system that can manage all hardware and software components from multiple vendors on a common AdvancedTCA blade platform, referred to as the *management and availability gap.*

The Managed Object Hierarchy (MOH) approach

A comprehensive AdvancedTCA element management architecture must enable administrators to monitor and manage the availability of all network components from the chassis, blades, and I/O boards to the operating system, middleware, and application software. By implementing a comprehensive element management architecture, administrators can quickly identify and address problems at the lowest level while streamlining Operations, Administration, and Maintenance (OA&M) activities, including configuring, provisioning, monitoring, diagnosis, recovery, reporting, and inventory management, accomplished through MOH.

> "The administrator wastes time attempting to isolate the source of the fault and may even send a component back to the TEM, only to have *no trouble found.*"

MOH is a SAF-compliant Java framework that provides a well-defined set of high-level carrier grade APIs that can be used with any operating system to create a robust element management system for AdvancedTCA blade platforms. MOH uses Java Management Extensions (JMX) technology to define each component and its relationship to all other components in the element management architecture. MOH-based element management systems provide the data needed to diagnose and isolate faults and even offer detailed repair instructions. Java's *write-once, run-anywhere* portability enables fast, easy integration of mixed hardware and operating system solutions in a common AdvancedTCA blade platform.

Sun Microsystems is using MOH in its AdvancedTCA blade platform, intelligently placing sensors in each layer (hardware, OS, I/O, and software) and mapping the telemetry information provided into usable models. By providing

this syntactically and semantically consistent element management architecture for every component of the AdvancedTCA system, MOH can reduce the need for heuristic coding by as much as 75 percent, significantly reducing time to market and implementation costs by as much as 30 percent. Figure 1 shows Sun's Netra CT900 ATCA Blade Server.

Figure 1

By taking advantage of Sun's innovative AdvancedTCA blade platform, which offers dual processor/core UltraSPARC and AMD Opteron blades (Figure 2) with a choice of carrier grade Solaris 10 and MontaVista Linux operating systems, TEMs can reduce their total cost of development and time to market while maximizing their return on investment.

Figure 2

With Sun's expertise in highly reliable carrier grade servers and operating system, advanced system management architecture, carrier grade high availability technologies, and end-to-end OEM service offerings, TEMs can rapidly deliver cost-effective, next-generation telecom services that bridge the management and availability gap, giving them a competitive edge in the highly competitive telecom equipment marketplace.

Raju Penumatcha *is vice president, Netra Systems and Networking. As a vice president, Raju is responsible for the Netra systems and Networking group within the Scalable Systems Group. His group has the charter to develop Netra Systems, Networking, Cryptography, and Fabric products and technology.*

Since joining Sun in 1988, Raju has significantly contributed to the growth of the Netra Systems and Networking group. His group has contributed more than 90 patents for Sun. He was also responsible for developing the fastest connectivity products (spanning from Fast/GbE to OC48 POS products) for Sun servers. His products helped Sun achieve the highest number of SSLOps through SSL and IPSec accelerator products and Raju drove migration of both Fast and GbE onto the server motherboards. He was instrumental in driving and delivering specialty Networking products, like Load Balancers and SSL Proxies, for Sun's Blade servers. Raju's current focus is on future-generation Netra servers for the Telco/NEP markets, 10 GbE, InfiniBand technology to enable clustering applications in the HPC space, Cryptographic offload solutions, and migrating some of these technologies onto Sparc processors.

Raju has a BS degree in Electrical Engineering from Bangalore University, India, and an MS degree in Computer Engineering from University of Michigan at Ann Arbor.

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Website: www.sun.com


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MIDDLEWARE

Company Name/ Model Number	Website/ Description	Carrier grade OS	Carrier grade Linux	Middleware
Accelent Systems	**www.accelent.com**			
e-micrOS	Sits between the OS and microprocessor including the accelBIOS core, accelTool SDK, and accelSys management tool • Product suite functions with Windows CE or Linux (acceLinux-Accelent's Embedded/ Mobile Linux) operating systems, and a number of ARM-based processors, including Intel's StrongARM and next-generation XScale microarchitecture • Core software and associated tools provide the custom boot loaders, OALs, and device drivers that allow OEM hardware to communicate with the operating system			•
Clovis Solutions	**www.clovissolutions.com**			
System Infrastructure SW Platform (SISP)	For using SISP in designing and implementing communication products and product platforms • Platform adaptation components help abstract platform-specific details from the applications and other SISP components, increasing application portability and scalability across platforms • Operating System Abstraction Layer (OSAL) • Hardware Abstraction Layer (HAL) • Transport Object (TO) • Database Abstraction Layer (DBAL) • Infrastructure core provides a completely distributed and hierarchical management operating environment			•
Commetrex	**www.commetrex.com**			
BladeWare	A telecom operating system • Consists of OTF Kernel telecommunications middleware (an OpenMedia media-stream framework), and IP-media technologies in a configuration specifically designed to allow the telecommunications OEM to easily develop a media server without the need for DSP resource boards • System expansion is accomplished by adding server blades rather than DSP resource blades • IP-only telephony: No need for specialized network interface boards • Runs on Solaris, Win32, and Linux			•
Continuous Computing	**www.ccpu.com**			
upSuite	A high availability platform software family • Interwoven software modules and APIs that provide middleware services for high availability telco applications • Provides a framework that allows users to port or create new, highly available applications that run on CCPU's open standards hardware platforms • Applications include carrier-class OAM&P platforms, VoIP media gateways, SS7 signaling gateways, and enhanced services such as conferencing and announcement servers			•
Enea	**www.enea.com**			
Element	Application Development Framework (ADF) and HA middleware • Suitable for distributed telecom, datacom, automotive, industrial control, and medical instrumentation • Provides communications services that make it easy to develop complex distributed applications spanning multiple processors and operating systems • Includes instrumentation, fault management, upgrade management, and shelf management services that make it easy to monitor, provision, service, upgrade, and fine-tune distributed networks			•

Continued on page 38

NEW PRODUCTS

WinSystems CompactFlash

Acqiris TC840 Time-to-Digital Converter

Kaparel AdvancedTCA Enclosure

More new products on page 41.

PRODUCT GUIDE

MIDDLEWARE

Company Name/ Model Number	Website/ Description	Carrier grade OS	Carrier grade Linux	Middleware
ESO Technologies	**www.eso-tech.com**			
HAPx	HA middleware providing fault recovery and system management services for computing/communication platforms • Suits applications that must guarantee service continuity, such as the 99.999 percent+ uptime carrier grade equipment requires • Available in two versions: HAP1: HA and System management for HPI based systems; HAP2: HA management for any system • Control and monitoring of applications, database, protocol stacks, HW resources • Stateless and stateful redundancy • HW and SW dependency management			•
GoAhead Software	**www.goahead.com**			
SelfReliant 4.0	Supports AdvancedTCA platforms including Intel's NetStructure Chassis, Kontron's VHDS, Motorola EndurX platform, RadiSys Promentum, and HP Advanced Open Telecom Platform • Includes support for PICMG 2.16 platforms and PCI platforms such as the Augmentix A+ series • Supports RAID 1 running on the Linux Multiple Device (MD) driver • SelfReliant MIB accessible via SNMP • Virtual IP addresses can be dynamically assigned and unassigned to the active resources in a system • Hot-swap management			•
SelfReliant 5.0	Integrate the HA middleware with hardware and software commonly used to create embedded solutions • Supports a variety of leading AdvancedTCA platforms including Intel's NetStructure Chassis, Kontron's VHDS, Motorola's EndurX platform, RadiSys Promentum, HP's Advanced Open Telecom Platform as well as PICMG 2.16 platforms, and PCI platforms such as the Augmentix A+ series • Provides integration with leading in-memory databases such as TimesTen's Data Server • SelfReliant MIB accessible via SNMP			•
SelfReliant 7500	System-wide logging mechanism • HAPx is easily portable to different OS/Platforms through its architectural features: C++ library linked with user application • Use of sockets, threads, events, and mutexes • Comprehensive set of application samples illustrates the use of the HA features • Included: HPI-Exerciser, a hardware event insertion tool for global testing of the HA platform behavior using hardware event triggering or simulation • A common Graphical User Interface (GUI) provides an intuitive and easy-to-use Web interface			•
MontaVista	**www.mvista.com**			
MontaVista Linux Carrier Grade Edition	A COTS Linux platform for telecommunications applications • Designed for edge and core telecommunications, including IP and voice networks, optical networks, signaling gateways, and VoIP gateways • HA features, including CompactPCI hot-swap drivers, redundant Ethernet, and RAID-1 • Hardened driver architecture • Resource monitoring and fault management • Incorporates standard interfaces for flexibility, portability, and longevity • Supports PICMG 2.16-compliant platforms, standard rack-mount systems		•	

MIDDLEWARE

Company Name/ Model Number	Website/ Description	Carrier grade OS	Carrier grade Linux	Middleware
Motorola	**www.motorola.com/computing**			
NetPlane Core Services Software	Service Availability Forum (SA Forum)-compliant HA middleware • First product in the NetPlane Software suite – a family of software products that provides an open, standards-based software execution environment • Designed specifically to meet the high availability needs of telecom and other industries that require a combination of computing power, high-performance communications, and always-on capability • Sold as part of Motorola's Avantellis series of communication servers			•
NetPlane Software	Family of open service availability software for next-generation platforms • Open, standards-based, platform-independent, and portable software execution environment for communications servers • Implements SA Forum HPI and AIS interface specifications • Scalable from small platforms to large, multiple-shelf systems • Includes an extensive range of protocol and application services • Helps equipment manufacturers reduce development costs and accelerate time-to-market			•
TimeSys	**www.timesys.com**			
Carrier Grade Linux 2.0 Upgrade Program	Upgrade of any 2.6-based PowerPC or x86 Linux distribution certified by TimeSys to a complete OSDL CGL 2.0 distribution within 30 days of joining the program • Ongoing access to the latest open source updates • Includes advanced tools to further customize CGL 2.0 distributions to developer specifications • Available for boards including Freescale reference boards, IBM reference boards, AMCC reference boards, Motorola boards, all x86 platforms supporting Linux, and more • Custom CGL 2.0 upgrade programs available for any hardware		•	
TimeSys Linux RTOS	A single-kernel Linux RTOS • Full Linux distribution based on kernel version 2.4.18 • Royalty-free real-time modules transform Linux into a true RTOS • Low-latency kernel • Full kernel preemption • Unlimited process priorities • Constant time scheduler • Priority schedulable interrupt handlers and SoftIRQs • High availability/carrier grade features • POSIX message queues • Unique priority inversion avoidance mechanisms • High-resolution timers • Complete set of more than 120 root file system packages	•		
UXComm	**www.uxcomm.com**			
ATCA Solution 1.0 – ATCA Management Software	Integration-ready software platform for AdvancedTCA system management • Discover: Discover servers and AdvancedTCA Chassis Management Modules (CMM) • Monitor: Customized displays for AdvancedTCA chassis inventory • Detect and Alert: Send notification through SNMP and e-mail for thresholded events • Failover: Provision replacement servers as needed • Customizable user interface: Deploy a single console for complex system • Software development suite: Extendable to meet the needs of your environment			•

ETXexpress Module with Intel® Pentium® M and Mobile Intel® 915GM Express Chipset

As the first member of the ADLINK ETXexpress family, the ETXexpress-IA533 uses low power Intel® Pentium® M processor 760 at 2.0GHz and the Mobile Intel® 915GM Express Chipset. Both the processor and chipset are part of the embedded Intel® Architecture that ensures a long production life for applications that need extended availability. The ETXexpress-IA533 supports dual channel DDR2 533MHz memory and comes with a single on-board Gigabit Ethernet port. In addition to the on-board integrated graphics, a Graphic PCI Express x16 slot is also available. The board connects up to four additional PCI Express x1 devices. The module has legacy support for 32-bit PCI and ISA through LPC.

For more info, go to:
www.adlinktech.com/products

Full-size Intel® Pentium® 4 (LGA775) Processor SBC

The new NuPRO-851DV has a high-computing capability. It supports an 800MHz FSB and Intel® Pentium® 4(LGA775) processor with Hyper-Threading technology. It has a large communication bandwidth with two PCI Express x1 Gigabit Ethernet ports. It supports Serial ATA for high-speed storage, USB 2.0 and other generic features including VGA, COM, keyboard, mouse and hardware monitoring.

For more info, go to:
www.adlinktech.com/products

6" Cube Multi-App Embedded Computer w/ Lots of Possibilities!

The GEME computer is powered by low-voltage fanless CPU making it ideal for embedded motion, vision, DIO, communication and high-speed link applications. It has an expandable enclosure designed for one PMC and up to three PC/104 modules. Integrated four-channel video capture supports NTSC/PAL cameras at up to 30 frames per second. The GEME is compact with frontal I/O access and multi-storage options.

For more info, go to:
www.adlinktech.com/products

High-Performance 3U CompactPCI Intel® Pentium® M / Intel® Celeron® M Processor SBC with Dual GbE on PCI Express

The cPCI-3915 CPU board is a 3U 4HP or 8HP system slot single-board computer with up to 2.0GHz for the Intel® Pentium® M CPU. This SBC is based on the Intel® 915GM chipset with 400 or 533 MHz FSB. One SO-DIMM socket carries up to 1GB 400/533 MHz non-ECC DDR2 RAM. The cPCI-3915 offers two Gigabit Ethernet ports, two RS-232 ports, one IDE ATA 100/66/33 port, one CompactFlash socket, two SATA-150 interfaces, quad USB 2.0, and a VGA/DVI interface. The Ethernet ports support PXE remote boot.

For more info, go to:
www.adlinktech.com/products

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PICMG 3.4 Advanced Switching Interconnect AdvancedTCA Processor Blade with Dual 64-bit Low Voltage Intel® Xeon™ Processors

The new aTCA-6891 processor blade features:

- PICMG 3.4 ATCA Advanced Switching Option3
- Quad ASI x4 Fabric Interface Channels up to 5- Slot Full-Mesh Configuration, 32Gbps
- Dual 64-bit Low Voltage Intel® Xeon™ 2.8GHz, 1MB L2 Cache, Hyper-Threading Processors
- Dual DDR2-400 REG/ECC Channels with 16GB max. Capacity
- Intel® E7520/6300ESB/6700PXH Chipset
- Dual 64-bit 33/66/100/133MHz PCI/PCI-X PMC with PIM
- RAID 0/1 SATA Support

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BLADES: STORAGE

Adtron Corporation
Website: www.adtron.com
Model: Bladepak SC6M RSC No: 30035

A storage blade that delivers self-contained RAID-1 functionality • Redundant disk storage, up to 80 GB in a 6U CompactPCI single slot • Configurations for either PCI or off board SCSI connection • Front panel hot swapping for replacement of a failed disk drive • Automatic rebuild of a new disk drive after operator initiation • Independent operation of redundant drives without host intervention featuring Adtron ActiveRAID technology • No additional software drivers are required for operation as a SCSI boot and data storage system

BRIDGE: OTHER

ATTO Technology, Inc.
Website: www.attotech.com
Model: FibreBridge 2390 RSC No: 25611

Fibre Channel-to-SCSI bridge featuring support for 4 Gb Fibre Channel and Ultra320 SCSI • One 4 Gb Fibre Channel port and two independent Ultra320 buses • Available as a 4U CompactPCI board or a desktop enclosure with rack-mount kit • Up to 280 MBps sustained data-transfer rate • SFP Fibre Channel Connector • Auto negotiates to 1 and 2 Gb Fibre Channel • Dual-stacked VHDCI SCSI connectors • Intelligent Bridging Architecture optimizes performance while allowing for value-adding applications to reside on the bridge • Full support for full-duplex Fibre Channel data transfers, direct connect to F-port fabric switches, FC-AL, PLDA, SNMP, Telnet, and FTP • 10/100 Ethernet with RJ-45 connector for local management and monitoring over LAN • Manual and auto LUN mapping allows for flexible management • Advanced diagnostics capabilities

BRIDGE: PROCESSOR-TO-PCI

Tundra Semiconductor Corporation
Website: www.tundra.com
Model: TSi109 RSC No: 30187

200 MHz 60x/MPX processor bus with dual CPU support and advanced pipeline architecture • DDR2 Memory Controller – up to 50% memory power savings compared to DDR • Integrated Clock Generator with optional Spread Spectrum capability • Designed for 200 MHz operation with only 8 PCB layers • Low latency non-blocking internal switch fabric • Pin compatible with Tsi108

CARRIER BOARD: PMC

Dynamic Engineering
Website: www.dyneng.com
Model: cPCIBPMC RSC No: 25578

The cPCIBPMC (CompactPCI to PMC) adapter/carrier converter card provides the ability to install a PMC card into a standard CompactPCI slot • The cPCIBPMC has a PMC card slot mounted to a universal 3U 4HP CompactPCI card • Suitable for 32/64 with 33/66 MHz bus operation • Size: 3U 4HP • PMC compatible slot: One PMC slot provided • Speed: a choice between the cPCI2PMC and the cPCIBPMC • With the cPCI2PMC direct connect to the PCI bus the latency to the PMC is optimized • With the bridged design of the cPCIBPMC the system speed is optimized • In some cases the possibility of doing 64-bit accesses to 32-bit PMC ports (memory) and 66 MHz primary PCI with a 33 MHz PMC secondary may be faster than the direct connect model

CHIPS & CORES: BUS INTERFACE

Integrated Electronic Solutions
Website: www.integratedelectronicsolutions.com
Model: IES5501 RSC No: 29594

Dual, bidirectional, unity gain two-wire bus buffer • Compatible with I2C bus (standard and fast mode), SMBus (standard and high power mode), and PMBus • Low input-output offset voltage • Threshold and offset parameters allow the connection of several devices in series • Low noise susceptibility • Enable pin allows bus segments to be disconnected • Wide range of bus voltages from 1.8 V to 15 V • No minimum bus capacitance requirement

DATA ACQUISITION

Acqiris
Website: www.acqiris.com
Model: DC152 Digitizer RSC No: 25636

Dual channel digitizer with 2 GHz of bandwidth that provides synchronous sampling of 2 GSps on both input channels with up to 256 Mpoints of optional acquisition memory; in single-channel applications this doubles to 4 GSps and up to 512 Mpoints • Up to 4 GSps sampling rate with 10-bit ADC resolution • Dual-channel 50-ohm front end with 2 GHz bandwidth, software selectable interleaved single-channel mode, on either input • Standard input option, with 2 GHz bandwidth, 50-ohm, DC or AC-coupled, with internal DC calibration • High-frequency input option, with 3 GHz bandwidth, 50-ohm, DC-coupled • Low dead time (350 ns) sequential recording with time stamps • Multi-purpose I/O connectors for trigger, clock, reference, and control signals • 3U single-slot compliant to both the PXI and CompactPCI standards • 2 GHz Auto-Synchronous Bus system (ASBus2) for trigger and clock signal distribution to multiple modules • High-speed PCI bus transfers data at sustained rates up to 100 MBps to host PC • Built-in high-resolution Trigger Time Interpolator for accurate timing measurements • Device drivers for Windows, LabVIEW RT, Wind River VxWorks, and Linux (support for other operating systems on request)

For more information

Enter the product's RSC# at www.compactpci-systems.com/rsc

DATACOM: SERIAL CONTROLLER

General Standards Corporation
Website: www.generalstandards.com
Model: CPCI-SIO4ARHM RSC No: 25713

The CPCI-SIO4ARHM and its transition module make a four channel full-duplex RS-422/485 serial board set • Each serial channel of the CPCI-SIO4ARHM can operate up to 10 Mbps in synchronous mode • Optional 32 KB FIFO buffer for both transmit and receive (256 KB total FIFOs) data on each channel provides for a smooth and efficient interface between the serial interfaces and the host computer • The board is based on the Zilog Z16C30 high-speed Integrated Universal Serial Controller (USC), which supports Asynchronous, Isochronous, Bisync, Monosync, HDLC, SDLC, External Sync, and Nine-Bit protocols • The USC chip provides full duplex operation with baud rate generators, digital phase-locked loop for clock recovery, and a full duplex DMA interface • One rear transition module is required and is priced separately • The module is available with RS-422/485 or RS-232 transceivers

DATACOM: ARCNET

Contemporary Controls
Website: www.ccontrols.com
Model: CPCI22 RSC No: 25764

Utilizes COM20022 ARCNET controller • Interfaces ARCNET with CompactPCI bus computers • Low-profile, 3U form factor • Hot swapping • Supports coaxial, fiber-optic, and twisted-pair cabling including EIA-485 • Automatic configuration of I/O and interrupt • High-speed I/O access to the COM20022 • Variable data rates up to 10 Mbps • Jumperless configuration • Plug-and-play • NDIS or null-stack Windows driver • Suitable with all MOD HUB and AI Series active hubs manufactured by Contemporary Controls • CMOS design for low-power consumption

DATACOM: GENERAL

EKF-ELECTRONIK GmbH
Website: www.ekf.de
Model: CG2-SHANTY GPS Receiver RSC No: 30181

CompactPCI based GPS receiver board, able to determine the velocity and to synchronize a system with the global time (UTC) • Often industrial computer systems need synchronization to a precise time standard • A solution to this problem would be any radio controlled clock • Unfortunately, most regions have their own local transmitter standards • Hence, for universal use (for example, if systems are mobile or destined for export), a GPS based clock is preferable • The CG2-SHANTY 3U Eurocard is provided with a high performance receiver engine continuously tracking all satellites in view for a time accuracy better than 1us and horizontal accuracy better than 3 m • The receiver is compatible with passive or active antennas and supports the NMEA-0183 data protocol, thus allowing nearly any GPS application program to be used with it

ENCLOSURE

VMETRO
Website: www.vmetro.com
Model: SANcab RSC No: 25291

A semi-rugged rack-mount storage cabinet • Multiple cabinet configurations available including disk storage only or disk storage with a VME or CompactPCI backplane to serve as a mechanical integration platform for complete recorder applications • Standard configuration is a four-slot 6U VME backplane and up to 12 disk drives • Configured as a storage device only and holds up to 18 shock-mounted Fibre Channel disk drives • Can be delivered with options for airborne power requirements such as 110V AC 400 Hz and 24 and 48 Vdc • Dual 2 or 4 Gbps Fibre Channel interfaces • Split backplane for dual loop operation • Up to 385 MBps sustained recording using Vortex recorders • Up to 5.4 TB capacity • 4U or 6U 19-inch rack-mount chassis

ENCLOSURE + CARD RACK + POWER SUPPLY

AP Labs
Website: www.aplabs.com
Model: FS-1280 Rackmount RSC No: 30156

Front-load, rugged, hard-mount chassis single or dual 8 slot – 19" (W) x 15.75" (H) x 18" (D); weight 85 lbs • Shock: MIL-STD-810, MIL-S-901D, Vibration: MIL-STD-167, EMI/RFI: MIL-STD-461• Hinged front door for easy card access; removable peripheral carrier in 8 slot single backplane version • Hinged front door for easy card access; removable peripheral carrier in 8-slot single backplane version • Available with CompactPCI backplanes • Front-to-rear airflow

Kaparel Corporation
Website: www.kaparel.com
Model: AdvancedTCA Enclosure RSC No: 30136

Rittal incorporates innovative components to produce reliably available systems up to Level 5 for AdvancedTCA and MicroTCA • Everything is fully assembled, ready to run and individually configured • And the same naturally applies equally for CompactPCI, VME, and VME64x • Case solutions in 5U, 12U, 13U, or cube design • Climate control concepts up to 200 W/board and more • High-speed backplanes up to 10 Gbps • Case solutions in 5U, 12U, 13U, or cube design • Climate control concepts up to 200 W/board and more • High-speed backplanes up to 10 Gbps variable • Rittal incorporates innovative components to produce reliably available systems up to Level 5 for AdvancedTCA and MicroTCA • Fully assembled, ready to run, and individually configured for CompactPCI, VME, and VME64x

I/O: ANALOG

KineticSystems Company, LLC
Website: www.kscorp.com
Model: CP213 RSC No: 30034

The CP213 is a single-width, 6U, CompactPCI/PXI module with 32 or 64 differential analog input channels that can be configured as 64 or 128 single-ended analog input channels • A 16-bit ADC scans each channel at a user-selected scan rate • Scans may be triggered from the internal clock, 1 of 8 PXI backplane triggers, the PXI star trigger bus, or an external SMB connector • The CP213 also has programmable gain, and channels 1 and 33 may

be configured as isothermal reference channels for temperature measurement apps • The CP213 also includes 16 Digital I/O channels that may be configured as Digital I/O or attached to a frequency in, counter in, or timer out channel

INDUSTRIAL COMPUTERS

Kontron
Website: www.kontron.com
Model: CP307 **RSC No: 30027**

A 3U CompactPCI with dual-core processor ideal for performance-hungry, high-availability, and robust industrial applications • PCI Express based, high density 4 HP or 8 HP CPU with passive cooling • Scalable processor speed, Intel Core Solo – Core Duo up to 2.0 GHz • Support of latest PSB performance with 667 MHz • Up to 4 GB DDR2 667 MHz SDRAM dual channel memory • 2x GbE interfaces via PCI Express plus dual screen graphics, DVI, and CRT • Latest I/O technology with up to six USB 2.0 channels and two SATA

MASS STORAGE: ATA

IEI Global Sourcing
Website: www.ieiworld.com
Model: ICARD-2140 **RSC No: 29528**

Support for up to 4 Serial ATA (S-ATA) drives • RAID-0, RAID-1, and RAID-0+1 improve the data performance and provide the data redundancy and rebuilding • Provides an inexpensive way for users to increase PC speed or fault-tolerance • IC chipset: Silicon Image Sil3114 • Supports RAID-0/1/0+1 • Serial ATA rate up to 1.5 Gbps • Serial ATA Specification 1.0 • Supports Windows and Linux OS • Supports PCI 2.2 specification

MASS STORAGE: RAID

Adtron Corporation
Website: www.adtron.com
Model: EA8R Bladepak **RSC No: 29662**

First in its class of carrier-grade storage blades, the EA8R provides sophisticated Adtron SmartStorage architecture and incorporates Adtron ActiveRAID in a standard Advanced Telecommunications Computing Architecture (AdvancedTCA) form factor • Adtron ActiveRAID Technology provides RAID-0 or RAID-5 capabilities • Using iSCSI over high speed GbE interface with the well-established SCSI command set permits the ability to manage data storage and retrieval with support for multiple hosts • Dual GbE Interface: Shelf redundancy; redundant ports on the backplane provide two paths to the storage blade • Enterprise-class 2.5-inch hard disk drives: High performance and provides 100% duty cycles in RAID operations

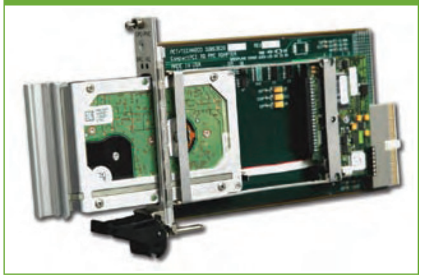
MASS STORAGE: SOLID STATE DISK

SiliconSystems, Inc.
Website: www.siliconsystems.com
Model: SiliconDrive **RSC No: 25601**

Advanced SiliconDrive storage technology engineered to meet the rigorous demands of the netcom, military, industrial, interactive kiosk, and medical markets • Suitable when replacing hard drives and flash cards or in host systems that require scalable, small footprint, or low power storage technology • Zero field failures from drive corruption • No forced product requalifications • Enhanced security features • Scalable technology • Real-time gauge of remaining usable life

MASS STORAGE: SATA

ACT/Technico
Website: www.acttechnico.com
Model: PMC ShuttleStor **RSC No: 30039**



Standard PMC mezzanine form factor IEEE 1386.1 • Uses standard parallel ATA drives • Onboard parallel to serial ATA conversion • SATA control logic supports hot swap • Off-the-shelf device driver support • One design is compatible with 1.8" to 7 mm ATA hard drives, and 2.5" to 9.5 mm ATA hard drives (Host board component height cannot exceed 2.5 mm for 9.5 mm thick hard drives) • Onboard hot plug power conditioning activity and hot swap indicators on the front panel

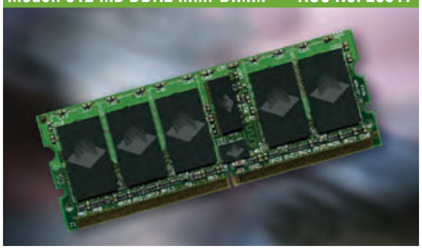
MEMORY: FLASH

WinSystems, Inc.
Website: www.winsystems.com
Model: CompactFlash RSC No: 25679

CompactFlash cards that operate from -40 °C to +85 °C • Provides industrial-grade reliability and industry-standard compatibility • Type I density up to 2 GB • True IDE mode capable and ATA-3 compliant • Offers high-performance 16.7 MBps burst • Onboard ECC • Industrial wear leveling • Spares and bad block management • > 2,000,000 program/erase cycles

MEMORY: GENERAL PURPOSE

White Electronic Designs
Website: www.whiteedc.com
Model: 512 MB DDR2 Mini-DIMM RSC No: 25317



512 MB of JEDEC-standard DDR2 Mini-DIMM • Designed for AdvancedTCA, CompactPCI, and VME applications • 64M x 72 DDR2 SDRAM high-density memory module consisting of nine 64M x 8 bit with four banks DDR2 Synchronous DRAMs in Fine Ball Grid Array (FBGA) packages, mounted on a 244-pin dual inline memory module FR4 substrate • Developed to overcome challenges experienced when using standard DDR SODIMMs, with ECC functionality • Enables space saving memory options to support a wide variety of applications such as Internet backbone switches, gateways, edge routers, embedded computing systems, and industrial control equipment • Features fast data transfer rates of PC-3200 and PC-4200 and clock speeds of 200 and 266 MHz • Includes differential data strobe option • Supports duplicate output strobe and Serial Presence Detect (SPD) with EEPROM

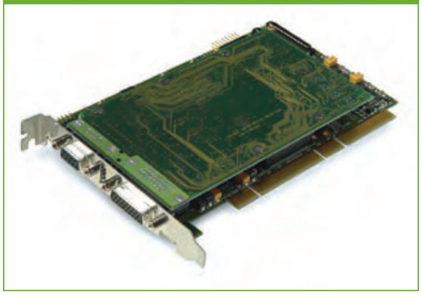
MEZZANINE: PRPMC

Embedded Planet
Website: www.embeddedplanet.com
Model: EP8343M RSC No: 30192

Freescale MPC8343E PowerQUICC II Pro processor at up to 400 MHz • Integrated hardware security engine with support for DES, 3DES, MD-5, SHA-1, AES, and ARC-4 encryption algorithms • Configurable memory options with up to 256 MB DDR RAM, 256 MB of flash, and 1 MB of NVRAM • Dual Gigabit Ethernet connections using the MPC8343E's integrated controllers for high-speed network applications • High speed USB 2.0 Host/Device/On-The-Go port using the MPC8343E's integrated controller • TransFlash connector supports up to 1 GB of removable storage in ultra small form factor • RS-232 serial port connector for direct module management and access to the operating system console • Onboard JTAG connection to simplify development and debugging of software applications

MIL-STD-1553

AIM-USA
Website: www.aim-online.com
Model: APX1553 RSC No: 25306



PCI-X compatible cards for MIL-STD-1553 test, simulation, and monitoring applications • Dual stream, dual redundant card (APX1553-1 is a single stream, dual redundant card) • Both are provided on a PCI-X compatible, short length card format • The APX1553 cards are available as Full Function, Single Function, and Simulator only versions • Onboard IRIG-B time code generator/decoder • Can monitor/stimulate up to eight discrete I/O signals • One or two 400 MHz Xscale processors for the Bus Interface Units (BIUs) • Additional 400 MHz Intel IOP80219 Application Support Processor • 1-4 MB Global memory is provided plus 128 MB Application Support Processor (ASP) memory • An onboard IRIG-B time generator/decoder is included having a sinusoidal output and free wheeling mode for time tag synchronization on the system level using one or more APX1553 cards • Full function driver software is delivered with the APX1553 cards for WIN2000/XP, Linux and a LabVIEW/VI/ LabWIN/ CVI interface to ease the customer integration task • The optional MIL-STD-1553A/B, PBA-2000/ ParaView Databus Analyzer/Visualizer Software (for Windows) can also be purchased for use with APX1553 cards

PROCESSOR: CELERON

Aitech Defense Systems
Website: www.rugged.com
Model: M586 RSC No: 25332

An ETX form factor CPU module based on the Intel Celeron Ultra Low Power 400 MHz and 650 MHz • The module is based on VIA CN400 + VT8237R chipset with integrated UniChrome Pro 3D/2D graphics and video controllers CRT/LCD interface and up to 64 MB video memory (SMA) • Integrates the VIA enhanced audio, 2 COM ports, 4 USB 2.0 ports, 1 EPP • Up to 1 GB DDR400 DRAM on SODIMM module, 10/100BASE-T Ethernet, primary and secondary IDE interfaces, keyboard and PS/2 mouse controllers, real-time clock, and watch dog timer

PROCESSOR: OPTERON

Performance Technologies
Website: www.pt.com
Model: CPC5564 SBC RSC No: 25554

The CPC5564 is the first 64-bit single slot CompactPCI single board computer designed for high-performance embedded applications, featuring the AMD Opteron 940 single core 2.2 GHz or dual core 1.8 GHz processor • 64-bit single or dual core processor support • Single slot high density compute blade • High-performance computing solution for PICMG 2.16 systems • 128-bit memory addressability to 8 GB, PC3200 DDR SDRAM with ECC • Onboard eight-port Gigabit switch • XMC/ PMC expansion port with support for 2x1000 Mbps Ethernet, eight lane PCI Express, and PCI-X 64/133 • CompactPCI hot-swap and IPMI BMC controllers • Supports both 32- and 64-bit operating systems: Linux x64, Windows XP x64, Solaris 9/10 x64 • Full compliance with PICMG 2.16 and 2.9 specifications

PROCESSOR: PENTIUM M

Acrosser Technology Co., Ltd.
Website: www.acrosser.com
Model: AR-B1891 RSC No: 29691

Pentium M single board computer with ATI Mobility Radeon 9000 for video gaming and high-end multimedia applications • Excellent performance • Low power consumption • Graphics capability • Ultimate security

Advantech Corporation
Website: www.advantech.com
Model: MIC-3390 RSC No: 30060

CompactPCI-based high-performance Intel Pentium M single board computer with PCI Express and IPMI 2.0-compliant interface • It is suitable for mission critical telecom and data communication applications where high availability is essential. The MIC-3390 CompactPCI 6U CPU board provides telecom equipment manufacturers (TEMs) with increased throughput and improved call-handling capabilities for applications at the edge of the network such as application servers, media gateway controllers, and home location registers • The MIC-3390 offers high-speed, low-power computing with support for the latest Intel Pentium M processors • Combined with the Intel I/O Controller Hub ICH6-M, this SBC supplies performance, connectivity, and throughput without compromising system thermal design

General Micro Systems, Inc.
Website: www.gms4vme.com
Model: C265 CONDOR **RSC No: 29531**

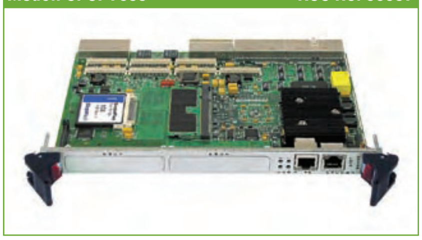
A high-performance, upgradeable Pentium M processor • Up to 2 GHz+ Pentium M processor with up to 2 MB of L2 cache • Field upgradeable CPU module to deploy latest Pentium M processors • Ultra-low power requirements as low as 12 W max • Highest performance per watt processor module available in the industry • Up to 1 GB of 266 MHz DDR SDRAM via SODIMM module • Dual GbE ports to front panel, rear, or PICMG 2.16 PSB • Dual video to support two DVI monitors or DVI and RGB simultaneously • One PCI-X compliant PMC module with rear I/O • Onboard support for one IDE HDD • One SAM I/O expansion module for audio, 1394, or other custom I/O • Full power management control • Four USB 2.0 ports and two serial ports • 512 KB of BIOS/user flash • RTC with field-replaceable battery • CPU temperature and voltage monitoring for safe operation • Fully hot-swappable 64-bit/66 MHz CompactPCI bus • Available in standard 0 °C to -55 °C or extended temperature -40 °C to +85 °C • Support for Windows XP/2000, VxWorks-Tornado II, and Linux • VME version available

SBS Technologies, Inc.
Website: www.sbs.com
Model: CR4 Pentium M **RSC No: 30059**

The rugged 3U CompactPCI single board computer with an Intel Pentium M LV 738, 512 MB DDR SDRAM, 512 KB Firmware HUB, two Gigabit Ethernet, available in convection-cooled or conduction-cooled configurations, can operate as system controller or peripheral card • Intel Pentium M LV738 processor 1.4 GHz • 512 MB DDR SDRAM • Type I CompactFlash on daughter card • Two Gigabit Ethernet ports • Two USB 2.0 ports • Two serial I/O (RS-232, RS-422) ports • Serial ATA port • Eight GPIO ports • Convection or conduction-cooled • System controller or peripheral card • Rugged 3U CompactPCI Single Board Computer with an Intel Pentium M Processor • 512 MB DDR SDRAM • Two Gigabit Ethernet ports, two USB 2.0 ports, two serial I/O (RS-232, RS-422) ports, and Serial ATA port • Type I CompactFlash on daughter card • Convection- or conduction-cooled • System controller or peripheral card

PROCESSOR: POWERPC

GE Fanuc Automation Americas, Inc.
Website: www.gefanuc.com/embedded
Model: CPCI-7055 **RSC No: 30057**



The CPCI-7055 is a single slot CompactPCI Single Board Computer (SBC) • IBM 750FX or 750GX PowerPC processor up to 1.0 GHz • The CPCI-7055 features the next generation Marvell Discovery III MV64460 chipset and offers up to 2 GB Double Data Rate (DDR) 400 SDRAM • Also features dual PMC sites (64-bit/66 MHz PCI-X, backward compatible to 5 V, 33 MHz PCI), up to 2 GB CompactFlash option, two high performance serial ports, and three 10/100/1000 Ethernet ports • PowerPC • 6U single slot SBC with up to 2 GB of DDR 400 SDRAM with ECC • Dual PCI-X (64 bit/100 MHz) PMC expansion sites • Features three Gigabit Ethernet connections, two serial ports, and up to 2 GB of CompactFlash • PICMG 2.16 (CompactPCI Packet Switching Backplane) and PICMG 2.9 (IPMI) compliant • Operating system support for VxWorks and Linux

PROTOTYPING AND DEBUGGING: FABRIC ANALYZER

FuturePlus Systems Corporation
Website: www.futureplus.com
Model: FS4410 **RSC No: 25570**

Serial RapidIO protocol analysis module • Low cost Serial Rapid IO protocol analysis • Full-size and half-size mid-bus probes with Soft Touch technology contacts available • Protocol decode software with Transaction Viewer included • Supports 8b encoded data at 1.25, 2.5, or 3.125 Gbps • Supports X1 and X4 lane widths • Lane deskew in x4 lane mode • Detects packet types and checks packet delimiters • Amplifies the capabilities of Analyzer by providing packet-aware data detection, filtering, and triggering • Supports debug of physical, transport, and logical layers (messaging, I/O, and streaming) • Probe manager software runs on a PC for real-time probe control • Optional FS4411 version supports both SRIO and PCI Express

SIGNAL CONDITIONER

Dataforth Corporation
Website: www.dataforth.com
Model: 8B49 & 8B39-07 **RSC No: 30021**

Model 8B49, a voltage output module, and model 8B39-07, a bipolar current output module, are additions to the Dataforth SensorLex 8B family • 1500 Vrms transformer isolation • ANSI/IEEE C37.90.1 transient protection • ±0.05% accuracy • High common mode rejection • Low drift with ambient temperature • -40 °C to +85 °C operating temperature range • 5 V power • CSA and FM certifications pending • CE compliant • Mix and match module types on back panel • Measures 1.11" x 1.65" x 0.4" (28.1 mm x 41.9 mm x 10.2 mm) • Suitable for embedded or portable applications such as mobile test stands, COTS military and defense applications, miniaturized security and surveillance systems, and embedded process control for semiconductor manufacturing equipment • Interfaces to almost any PC/104, CompactPCI, VMEbus, PXI, or proprietary data acquisition system board

SYNCHRO-TO-DIGITAL

Acqiris
Website: www.acqiris.com
Model: TC840 **RSC No: 30019**

Time-to-Digital Converter (TDC) module • Wide range, single- and multi-start • 50 ps timing resolution • Designed specifically for use in large scale experiments, including hydrodynamics, particle accelerator timing, nuclear fusion studies, and explosive testing, time-of-flight measurement in mass spectrometry

North Atlantic Industries
Website: www.naii.com
Model: 8810A **RSC No: 25738**

An upgrade to the 8810 instrument • New synchro/resolver angle measurement instrument, model 8810A, directly replaces the older 8810 • A full-function instrument capable of performing most synchro/resolver evaluation, calibration, and test

functions on components, assemblies, and systems • Fully independent dual-inputs • High-resolution touch screen controls • 0.001° resolution/0.004° accuracy • Autoranging inputs • Optional 2.2 VA reference supply • LXI compatibility • 47 Hz to 20 kHz operating frequency • Auto-phase correction • Interface compatibility with Ethernet, USB, IEEE-488, and parallel ports • Automatically accepts and displays input voltages from 1.0 to 90 VL-L and reference voltages from 2 to 115 Vrms over a broad frequency range of 47 Hz to 20 kHz

SYSTEM BOARDS

AAEON Electronics, Inc.
Website: www.aaeon.com
Model: PCM-8300 RSC No: 25646

Supports Intel Pentium M/ Celeron M Series processors • Supports 36/18-bit LVDS TFT panels • Supports two DDRII 400/533 SODIMM memory modules up to 2 GB • Dual PCI Express Gigabit LAN • 5.1 CH AC-97 2.3 codec With S/P DIF Function • One mini PCI socket for expansion modules • 4 USB 2.0, 4 COMs, Digital I/O

THERMAL MANAGEMENT

New Age Fans
Website: www.newagefans.com
Model: BFT192B RSC No: 30102

Provides an efficient method of cooling open architecture card cages on an individual basis • Low wattage, dual alarm, low noise, UL, patent pending • 2U high 19-inch rack-mount • Adjustable depth • Fire retardant, corrision resistant • Individual 12 V power supply • Full set of accessories • Simple installation

TURNKEY SYSTEM

Inova Computers, Inc.
Website: www.inova-computers.de
Model: ICPe-SYSC-EXP RSC No: 30152

3U CompactPCI Express System • 100 W CompactPCI Express 115 V/230 V AC/DC PSU 6-slot CompactPCI Express backplane with legacy support • Translation board with Gigabit Ethernet and HD interface Windows XP Embedded • MTBF > 200,000 hours 0 °C to +60 °C operational temperature • Conforms to EN50155 (DC PSU) 1 GHz ULV Celeron M /2.0 GHz Pentium M CPU • Intel 915GM chipset with DirectX 9 H/W support • Up to 2 GB 533 MHz DDR2 RAM VGA / DVI / TFT supported video formats • Up to 2048 x 1536 pixel video resolution • Up to two independent Gigabit Interfaces • Up to eight USB 2.0 Interfaces • CPU extension with HD, COM, and PS-2 interfaces • Single-slot, Inline Serial ATA Interface • uDOC Technology or CompactFlash • µController for System Management Intelligent Rear I/O • The conduction-cooled 1 GHz Celeron version is just 4HP wide and is suited to applications in harsh environments or extremes of temperature.

For more information, enter the product's RSC# at www.compactpci-systems.com/rsc

SBS Technologies, Inc.
Website: www.sbs.com
Model: AVC-CPCI-6000 RSC No: 30153

Advanced Vehicle Computer • Based on CompactPCI 6U system • Eight CompactPCI slots • 450 W rugged power supply • PowerPC based SBC • Flexible I/O options

CompactPCI® and AdvancedTCA® Systems

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